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CROSSBAR NANOCOMPUTER DEVELOPMENT

ALBANY COLLEGE OF NANOSCALE SCIENCE AND ENGINEERING, STATE UNIVERSITY OF NEW YORK AT ALBANY

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FINAL TECHNICAL REPORT

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14. ABSTRACT
This effort expanded development of memristive nanoelectronic junction materials for high density memory and advanced logic applications. The focus of the effort was to develop metal oxide materials for resistive memory devices (RMDs), which are also known as memristors or resistive random access memory (Re-RAM or RRAM). The major goal was to fabricate such devices in a crossbar configuration (overlapping metal lines which create multiple junctions in an array format) which would enable ultra high density arrays of devices. These arrays could eventually be used for high density memory applications, or could replace transistors in conventional CMOS architectures. The deliverable for this effort was to demonstrate a 2 x 2 crossbar structure (4 crossover points) that could be tested and compared to simulations which were performed in parallel. Our efforts on this project resulted in successful materials selection of high-performance metal oxides, development of the 2 x 2 crossbar (and even a 12 x 12 crossbar) array, and successful modeling of resistive memory circuits.

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1. Summary

This effort expanded development of memristive nanoelectronic junction materials for high density memory and advanced logic applications. The focus of the effort was to develop metal oxide materials for resistive memory devices (RMDs), which are also known as memristors or resistive random access memory (Re-RAM or RRAM). The major goal was to fabricate such devices in a crossbar configuration (overlapping metal lines which create multiple junctions in an array format) which would enable ultra high density arrays of devices. These arrays could eventually be used for high density memory applications, or could replace transistors in conventional CMOS architectures. The deliverable for this effort was to demonstrate a 2 x 2 crossbar structure (4 crossover points) that could be tested and compared to simulations which were performed in parallel. Our efforts on this project resulted in successful materials selection of high-performance metal oxides, development of the 2 x 2 crossbar (and even a 12 x 12 crossbar) array, and successful modeling of resistive memory circuits.

2. Introduction

The emerging revolution of nanotechnology is expected to stimulate enormous improvements in IT capabilities. Computer architectures are high on the list of technologies that will benefit from nanoscale breakthroughs in the structures, properties, and performance of microelectronics. For example, the critical feature size of Si-based, field-effect transistors has dropped below 50 nm, and yet continued reduction in transistor dimensions is expected as new nanomaterial capabilities as well as new nanoscale-centric circuit architectures are developed. However, the emerging trend in IT-focused nanotechnology development is one that looks beyond conventional CMOS technologies. It has become increasingly apparent to the IC community that the fundamental road blocks for continued enhancement of traditional approaches to transistor scaling and interconnects are rapidly being approached. Therefore, finding new computer architecture constructs – inventing and developing novel switching, memory, and interconnect technologies for processing information as well as "bottom up" based approaches to fabrication – is central to addressing the fundamental roadblocks facing IC technologies. It is anticipated that novel, nanotechnology-based, approaches to switches and interconnects will initially be implemented in conjunction with prevailing CMOS architectures. However, the full development of nanotechnology-based post-CMOS logic and memory elements are expected to result in major shifts in IC technology and redefine improvements in commercial and military information systems in ways that are anticipated to far surpass conventional CMOS. This research proposal explores such a novel, high-payoff, nanotechnology-based switch/interconnect paradigm based on crossbar nanoelectronic logic elements employing the recently demonstrated phenomena of memristance [1], an enabling new nanotechnology phenomenon that is being heralded as the fourth fundamental circuit element.

Memristive nanoelectronic devices share many of the properties of resistors, as well as the same unit of measure (ohm). However, in contrast to ordinary resistors in which the unit of resistance is permanently fixed, memristance may be programmed or switched to different states based on the history of the voltage applied to the memristance nanomaterial. This gives the memristor a hysteresis property in its I-V characteristic. This can be contrasted to ordinary resistors where there is a linear relationship between current and voltage. While similar hysteresis properties have been demonstrated by magnetic materials, these require the presence of large magnetic fields for implementation, which has proven to be a practical limitation to their utilization. Areas such as neuromorphic computing, signal processing, arithmetic processing, and crossbar computing are only some of the potential application areas of memristor nanomaterials. This effort proposed to collaborate with researchers at AFRL/RI to explore the synthesis, nanofabrication, and characterization of nanomaterial-based memristive devices.

Crossbar computer logic architectures are complex matrices of interconnected nodes that show great promise for scalability, size, weight and power issues. In their simplest form,

crossbar junctions consist of two nanowires (less than 100nm wide) that physically "cross" each other. The junction between these nanowires is composed of a junction material with tailored transport properties. Crossbar logic elements enable massively parallel computations with the potential for a reduction in power consumption and size by up to 2-3 orders of magnitude. Crossbar computing is also tolerant to hardware defects, due to its intrinsic, network-on-chip flexibility to re-route around defects. Preliminary efforts in crossbar computing have been demonstrated by researchers at Hewlett-Packard Laboratories, in which memristive elements were used.

3. Methods, Assumptions and Procedures

Modeling

Modeling and simulation were performed by co-simulation of the memristor model that was written using Verilog-A and an HSpice circuit simulator. Compact models were developed, and the memristor was modeled as a bipolar switching device. Two behavioral models were developed based on the type of electrical signal mode used to switch the device: voltage sweep mode and voltage pulsed mode. The sweep mode model of the memristive device was coded using the electrical parameters taken from electrical measurements of individual devices. The parameters were also obtained from piecewise linear approximation of its I-V curves. However, the pulsed mode model was coded using electrical parameters taken from the literature, as the pulse mode capability of the laboratory was being set up at the time.

Substrate preparation and thin film synthesis

The starting substrates for this effort consisted of 300 mm wafers on which $SiO_2/Si_xN_y/Si$ layers were deposited using standard chemical vapor deposition techniques. For the materials development and testing studies, Cu/Ta/TaN was deposited on the starting substrate by physical vapor deposition (PVD) as the electroplating seed, adhesion layer, and diffusion barrier, respectively. To form the Cu bottom electrode (BE), 1 μm of electroplated Cu was deposited onto the Cu seed layer. Chemical mechanical planarization (CMP) was then used to level and polish the plated Cu, smoothing the electrode surface. This Cu film served as the BE for all devices used in the development study.

Three different metal oxide films were synthesized onto the Cu BE using thermal oxidation, physical vapor deposition and atomic layer deposition (ALD). 1) TiO_x films (100 nm thick) were deposited by RF sputtering at 200W forward power on an unheated chuck: a) in a 4.2 mTorr argon atmosphere and b) in a 4.2 mTorr argon atmosphere with an 0.1% oxygen partial pressure. These process conditions yielded a nominal deposition rate of 0.08 nm/sec.2) HfO_x films were deposited by ALD with a chuck temperature of 250 ˚C and a chamber pressure of 0.19 torr. Process gases used were tetrakis(dimethylamido)- hafnium(IV) as the metal-organic precursor, and a 300 W RF O2 plasma as the reactant. The target thickness of HfO_x was 50 nm. 3) Copper oxide was synthesized by oxidation (thermal and plasma) and reactive sputtering. Thermal oxidation of the copper electrode was performed at 200-400°C in air at atmospheric pressure. Plasma oxidation was performed at RT and 280°C with an oxygen flow rate of 1-14 slm, a pressure range of 0.5-2.5 Torr, and an RF power range of 300-1000 Watts. Copper oxide was deposited by room temperature reactive sputtering at $1x10^{-2}$ Torr and 2000 W; the oxygen flow rate was maintained at 20 sccm, while the argon flow rate ranged from 3.5-20 sccm.

Device fabrication (for materials development/testing)

The top electrodes (TEs) for the development study were patterned using either a shadow mask or a conventional photolithography-based lift-off process. Au, Ni, Al, or Pt were deposited individually by electron beam evaporation to a final thickness of 100 nm. The resulting contacts ranged in size from 25-100 μm. For Cu_2O devices, "mesa" structures were fabricated by removing the excess Cu_2O that was not covered by the TEs. This was done through acid-based wet chemical etching of the oxide.

Crossbar fabrication

The starting substrate for this effort consisted of SiO_2/SiN/Si substrate described above. The first generation crossbar devices were fabricated using a damascene copper via process. Vias were etched into the SiO_2 layer using optical lithography and a reactive ion etch process. Cu/Ta/TaN was deposited by physical vapor deposition (PVD) into the vias, to act as a diffusion barrier and a seed for electroplating. Copper was then electroplated into the vias and chemical-mechanical planarization (CMP) was used to remove the Cu overburden and planarize the wafer surface. The HfO_x layer was deposited using the ALD parameters from above; the target thickness of HfO_x was 50 nm. Second generation crossbar devices were fabricated utilizing a similar SiO_2/SiN/Si starting substrate. The bottom Cu electrodes were no longer based on a via-based process and instead were defined using electron beam lithography. The HfO_x for this generation crossbar was deposited by room temperature PVD to stop the Cu from migrating into the overgrown HfO_x. For both crossbar generations, the top electrode fabrication was performed using electron beam lithography. More details regarding the fabrication of these crossbars is included in section 4.4.

Film and device characterization

Xray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) were performed for depth profiling and chemical analyses. Scanning electron microscopy (SEM), atomic force microscopy (AFM), and transmission electron microscopy (TEM) were employed to analyze the microstructure of the resulting films. X-ray diffraction (XRD) was utilized to determine the phase(s) present. Switching characteristics were investigated using sweep based current voltage (I-V) electrical measurements on an Agilent B1500A semiconductor parameter analyzer. Samples were mounted on a Cascade M150 vacuum chuck probe station, and contacted with W probes attached to Cascade DCM208 micro manipulators.

4. Results and Discussion

4.1 Key Accomplishments

As described above, this project focused on several key areas, including 1) modeling and simulation of crossbar/memristor circuits, 2) development of metal oxide materials for memristive circuits, and 3) fabrication of a prototype 2 x 2 crossbar device. The following results and discussion section describes, in detail, how each of these tasks was performed, and the key results that were generated.

The specific tasks of the project included:

4.2 Memristive crossbar nanocircuit modeling and simulation

4.3 Materials development and testing
- 4.3.1 Metal oxide materials evaluation
- 4.3.2 Evaluating the influence of copper on device properties
- 4.3.3 Alternative metal oxide fabrication methods development

4.4 Fabrication and testing of a prototype 2 x 2 memristive crossbar logic element
- 4.4.1 Fabrication of crossbar devices
- 4.4.2 Evaluation of device performance

4.2 Memristive crossbar nanocircuit modeling and simulation

Rationale:

Memristive devices offer a multitude of applications in computing. For example, ITRS recommends that redox-type memristors should be the subject of increased research/commercial development efforts to replace or supplement the current memory technologies, SRAM, DRAM, and Flash, as they approach their scaling limits [2]. Other applications that memristive devices are suited for include FPGA [3], encryption [4], and neuromorphic computing [5].

Therefore, an understanding of how a novel device, like the memristor, behaves and performs in conjuction with other devices, like CMOS, is crucial in assessing the device's performance and functionality in those architectures and circuits. This can achieved by developing models and by performing simulations. Modeling and simulations can also serve as a guide in the fabrication

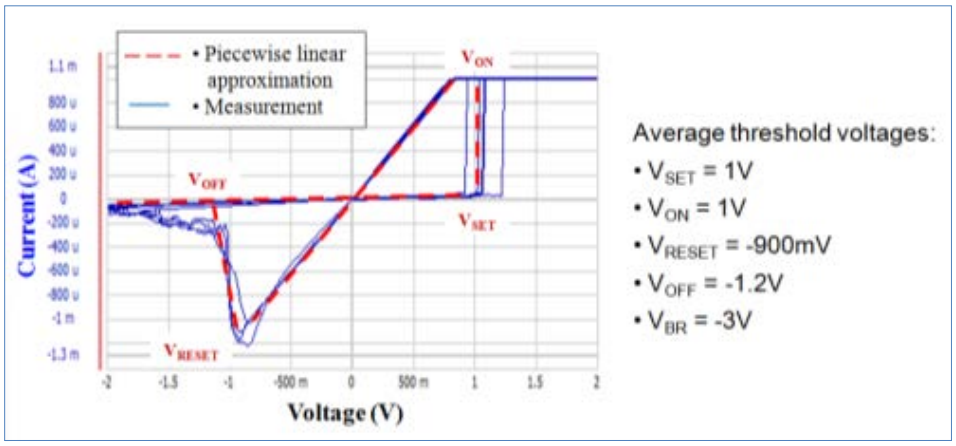
and design efforts. They can provide a better understanding on the impact of parameters such as material choice, memristive junction configuration, and device dimensions on performance.

Results:

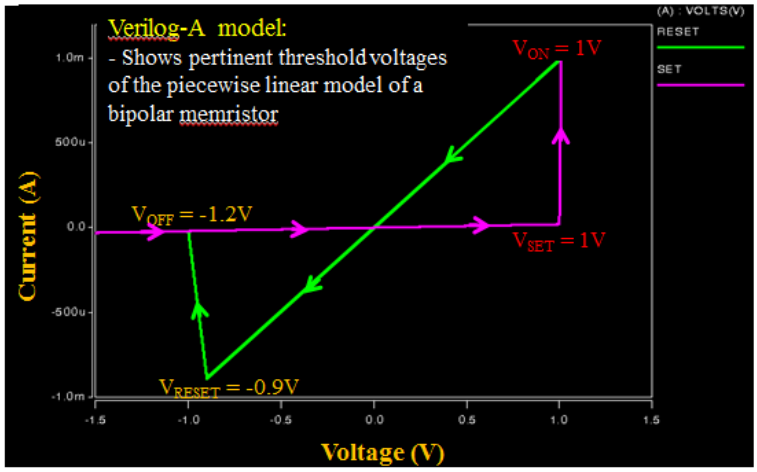
Sweep mode model

The sweep mode model that was written in Verilog-A discussed above was verified using an HSpice simulation of an individual memristor. Next, it was compared with data from an actual circuit.

As discussed above, the behavioral model for sweep mode was taken from electrical measurements of individual memristive devices, with its I-V curves approximated with piecewise lines (Figure 1). These parameters were then encoded into the Verilog-A model to replicate the I-V characteristics of the device operated in sweep mode. Figure 1 shows the I-V curve of the model from the HSpice simulation of the individual device when also provided with a sweeping voltage. It can be seen that the simulation I-V curve replicates that of the linearly approximated I-V curve from measurements, with the correct threshold voltages that were encoded into the model. This shows that the model can then be used to simulate the memristor with other electrical components, such as transistors, in a bigger and more complicated architectures properly using HSpice.



(a)



(b)

Figure 1: HSpice model validation of the sweep mode model written in Verilog-A. (a) shows the sweep mode measurements taken from an individual device and its corresponding piecewise linear approximation, while (b) shows the HSpice validation of the sweep model model written in Verilog-A.

Pulse mode model

The sweep mode model was created to replicate the full IV profile of a memristive device. In theory, there are an infinite number of states between the minimum and maximum resistance value afforded by a memristive device. In practice, one will not want to merely cycle a device, but stop at certain states, or resistance values, along the way. In the case of CMOS, memristive devices would be driven by pulses not DC sweeps. In light of these, a new model had to be created to account for an arbitrary pulse height and duration.

Due to the lack of empirical data, it was necessary to appeal to memristive device theory to develop the model. Memristance relates charge to flux. It is then natural to surmise, that the switching event may be triggered by satisfying an electric flux threshold, as opposed to meeting

a threshold voltage. In such a model, a switching event threshold for electric flux, the time integral of the applied voltage, was set and the history of applied voltage and duration was compared to this threshold. Once met, the model set the device. In a similar manner, though using the opposite voltage polarity, the device would reset.

To reiterate, the sweep mode model operated upon a threshold voltage switch mechanism, since the applied signal was supplied with the intent to fully set or reset the device. Under an arbitrary pulse scheme, this method could not readily be applied. Thus, based upon the flux threshold switching hypothesis, a low voltage pulse of long duration, a high voltage pulse of short duration, and a medium voltage pulse applied repeatedly were all capable of transitioning the memristive device to the low resistance state provided the flux threshold was attained. Figure 2 shows the results of a Matlab model simulation of a set operation for a single pulse, a) - c), and a pulse train, d) - f). In particular, for single-pulse programming, only two resistance states, HRS and LRS, are observed in the IV plot, a); for a pulse train, multiple intermediate states are observed in the IV plot, e).

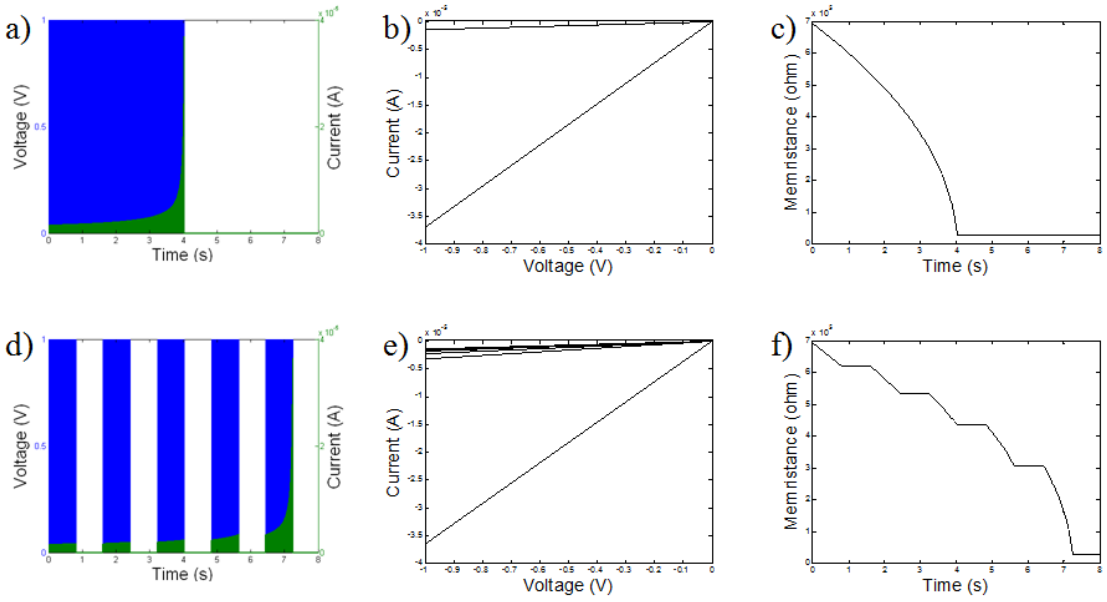


Figure 2: Matlab simulation results of a set operation via a single pulse, a)- c), and a pulse train, d) - f).

It is this repeated pulse programming that required additional thought. In the sweep mode model, there were two resistance states to operate at, LRS and HRS. For the pulse mode model, the simulated device had to be able to achieve intermediate states. As a proof-of-concept, a piece-wise linear model was employed where resistance of the memristor would change in a linear fashion. Such an approach was supported by the few pulse-operation papers available in the literature [6-7]. As the resistance approached its maximum value, the overall change upon device

behavior was minimal; whereas, for a device approaching the minimum value, the decrease in resistance was very gradual before reaching the lower limit abruptly. Such behavior is generally consistent with a linear resistance change.

In the end, the operational parameters of this model included the minimum and maximum resistance values and the threshold flux value for both set and reset operations. An example voltage and pulse duration to effect a set and reset were included to determine the rate of resistance change per time step of simulation.

As with the sweep mode model, the pulse mode model was translated into Verliog-A to run in HSpice. Two simulations were performed. The first one was to show the effect of providing pulses would fully switch the device from the HRS (maximum resistance) to LRS (minimum resistance). The second one was to show the effect of providing an arbitrary set of pulses that would enable partial switching. Figures 3 and 4 are comprised of three graphs each, in which the first graph shows the voltage pulse applied, the resulting current response is the shown in the second graph, and the change in resistance over time is shown in the third. Figure 3 shows the switching response of the device when provided with set and reset pulses and also read pulses to check the resistance state after switching. As also mentioned, these pulses should be sufficient enough to completely switch the device from HRS to LRS. As can be seen for set, the resistance abruptly decreases as it reaches the threshold and then gradually changes to the LRS at the end of the pulse. Reset is triggered as the negative threshold voltage is reached. A linear change of resistance is then seen as it goes from LRS to HRS. The read pulse provided after each switching didn't trigger further resistance changes and shows the resistance state after the switching process. Figure 4 then shows that response of the device when biased with a shorter, 50ns pulse, instead of the 110 ns pulse in Figure 3. As the resistance plot at the bottom of Figure 4 shows, the resistance starts off in HRS and once triggered with the voltage pulse, the device begins to decrease in resistance towards the LRS. The short pulse is only able to reduce the resistance to an intermediate resistance level between HRS and LRS, $R_{intermediate}$. By providing another set of pulses which completes the required flux, the final resistance, R_{on}, was achieved. Proceeding from LRS to HRS afterwards shows a similar trend: several pulses are needed to completely switch the device from LRS to HRS.

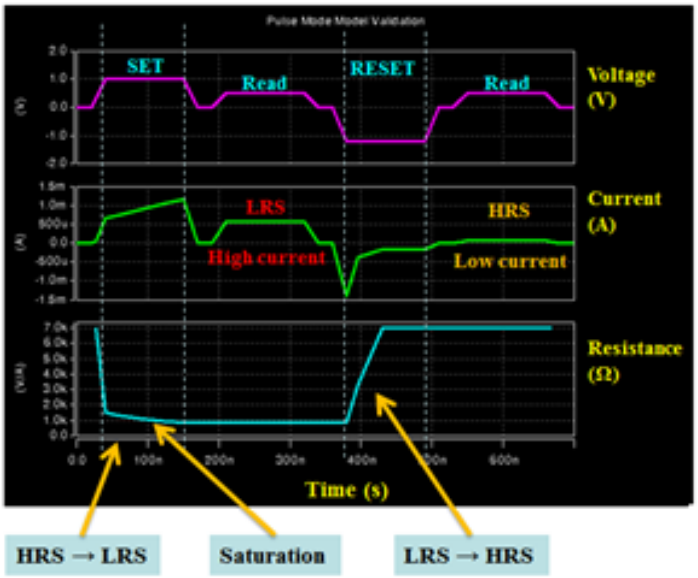


Figure 3: Pulsed mode model demonstration of full cycle memristive switching using Verilog-A and HSpice, where V_{SET} = 1V, V_{RESET} = -1.2V, t_{SET} = t_{RESET} = 110ns, R_{SET} = 3kΩ, and R_{RESET} = 7kΩ.

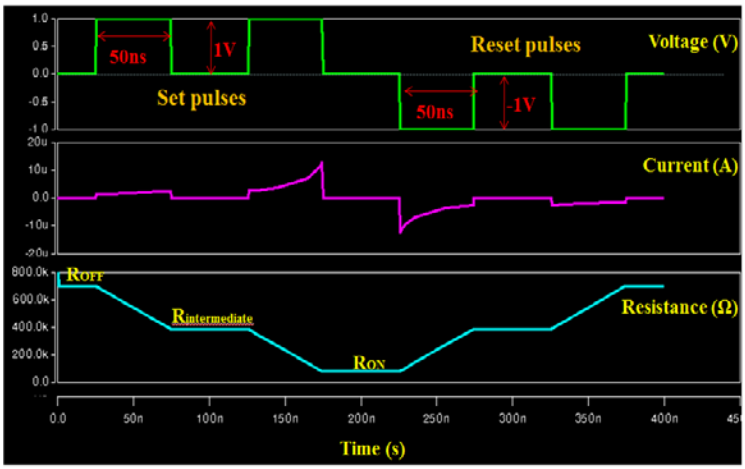


Figure 4: Pulse mode model demonstration of switching via multiple pulses, in this case two, to effect a full set or reset operation.

The pulse mode memristor model highlighted several issues that would need to be addressed. In the first, repeated DC sweeps at sub-switching voltages did not cause devices to switch as the electric flux threshold for switching events hypothesis predicted. Rather, the devices did appear to have a threshold voltage requirement. Additionally, the change in resistance in fabricated devices was not linear but rather abrupt. Numerous intermediate states as predicted in the model are rarely observed in practice.

Conclusions from Memristive crossbar nanocircuit modeling and simulation:

Developing memristor models for circuit simulations is important in the design of large-scale systems in order to assess its functionality and performance. We have employed behavioral modeling by approximating the I-V characteristics of actual memristive devices using piecewise linear curves and then taking the electrical parameters from them. The models are then encoded using the Verilog-A hardware description language, which was then linked to HSpice during circuit simulations. Two models, sweep mode and pulsed mode, were developed. Only the sweep mode model was validated and compared using both the simulation and actual measurements. It was shown that the sweep mode model effectively replicated the I-V characteristics of the curves taken from actual measurements. The pulse mode model, even though not validated yet through actual measurements, provided an insight on how the device may behave when stimulated using pulsed signals. For flux dependent switching devices, the model showed that full switching of the memristor is accomplished when provided with sufficient voltage and time to switch, otherwise, only partial switching is achieved.

The current models are still quite simple, and a lot of improvements still need to be done. In the future, it will be good to use the models to simulate larger systems and assess how well it performs. The models can also be updated to include other effects such as temperature. In doing such, the model can encompass a wider range of operation. Empirical models are quite useful when the physical mechanisms governing the memristor are not well understood; however, it will be better to incorporate the physics of the devices once available. While physical models can improve the accuracy of the simulations, the associated computational costs might limit its use in larger circuits. Therefore, this trade-off should be considered when choosing the appropriate model to use.

4.3 Materials Development and Testing

4.3.1 Metal oxide materials evaluation

Rationale:

Metal oxide based resistive memory devices can be fabricated using a wide array of metal oxide insulator/metal electrode combinations. To date, few studies have rigorously compared devices fabricated from multiple electrode/insulator combinations. Those studies that have compared devices with different electrode/insulator combinations show that the choice of electrode plays a large role in the switching characteristics of the resulting MIM devices. Kim, *et al.* used several different metal TEs for TiO_x–based devices, including Pt, Au, Ni, Al, and Ti [8]. When using Pt and Au electrodes, both bipolar and unipolar switching was observed, but Ag

devices exhibited only bipolar behavior. Further, devices fabricated with Ti TEs were not able to be switched, while Ni and Al TEs resulted in unstable switching behavior. Similar trends were observed by Vallee, *et al.* for HfO_x-based devices in which the switching behavior for Pt TEs was superior to Au and $WSi_{x(x>2)}$-based TEs [9]. Another study using HfO_x-based devices showed that the conductivity of the low resistance state (LRS) was related to the choice of TE material, and the heat of formation for oxidation of that material [10].

Clearly, the choice of metal oxide and electrode materials for resistive memory devices is important for their resulting electrical behavior. In this study, we chose to investigate several metal oxide/electrode combinations in an attempt to gain a broader understanding of their effects on resistive switching behavior. Cu_2O, HfO_x, and TiO_x oxides were formed on copper BEs, followed metallization with four different TEs (Ni, Au, Al, and Pt). Current-voltage measurements were then performed to characterize the switching behavior (unipolar, bipolar, non-polar), resistance ratio (R_{OFF} vs. R_{ON}) and approximate set/reset voltages.

Results:

TiO_x devices exhibited a wide range of electrical characteristics which were dependent upon both the TiO_x deposition method used and the TE material. In general, TiO_x deposited in an Ar-only atmosphere yielded devices with more repeatable switching behavior than TiO_x deposited in an Ar/O_2 atmosphere. In particular, devices deposited in an Ar/O_2 atmosphere with Al and Ni TEs exhibited diode-like behavior and could not be switched from HRS to LRS. Devices fabricated with Au and Pt TEs yielded the most consistent performance for both the Ar and Ar/O_2 deposition conditions. These devices had similar resistive switching properties with set voltages of ~0.7 V, reset voltages less than -0.4 V, and R_{OFF}/R_{ON} ratios of $\sim 10^6$. Interestingly, devices with Al and Au TEs exhibited unipolar switching behavior (turn-on and turn-off in the same voltage polarity) while devices with Ni and Pt TEs exhibited bipolar behavior (set and reset with opposite voltage polarity). Characteristic IV curves from TiO_x devices with Ni and Al TEs are shown in Figure 5.

Our devices behaved differently than those described in previous studies using TiO_x as the metal oxide. Kim *et al.* [8] reported both unipolar and bipolar behavior for Pt and Al TEs, while we observed only unipolar behavior for Al and only bipolar behavior for Pt. This group further showed that Ni and Al TEs yielded devices with unstable switching behavior, while we had mixed results for these electrode materials, partially dependent upon the deposition conditions of the TiO_x. Some of these differences may be due to the fact that Kim's devices used Pt BEs, while Cu BEs were used in our devices. Since the BE material was not varied in our experiments, however, we cannot determine the overall effect it has on switching behavior.

A distinguishing feature of the TiO_x-based devices was contact bubbling and delamination (see inset in Figure 5, right side). This phenomenon is well documented by

multiple research groups [11-12] and has been suggested to be the result of oxygen released from the bulk TiO_x. Contact bubbling was most pronounced when Au was the TE. Ultimately, contact bubbling will limit the integration of TiO_x-based memory devices with CMOS systems if this issue is not addressed.

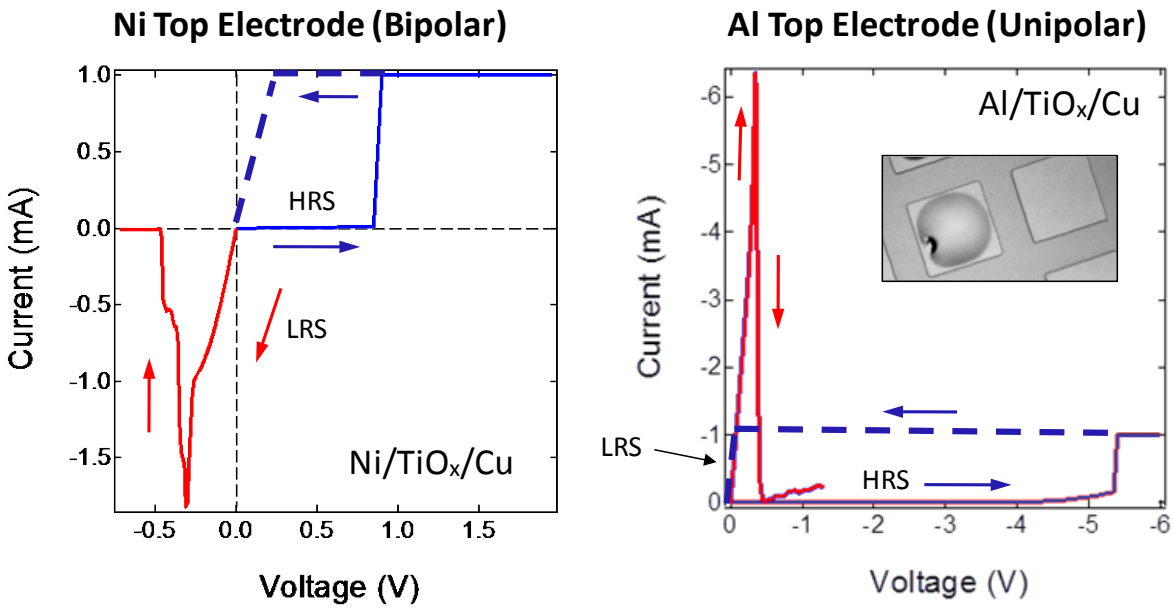


Figure 5: Current-voltage plots showing both bipolar (left) and unipolar (right) switching behavior for TiO_x devices. Bipolar behavior was observed when Ni top electrodes were used, while unipolar behavior was observed for devices with Al top electrodes. Top electrode bubbling and delamination (right, inset) was observed for all TiO_x devices, regardless of top electrode material.

HfO_x-based devices exhibited non-polar switching behavior independent of the TEs and without the need for a forming voltage. Non-polar behavior was exhibited by the ability to switch in both a unipolar and bipolar manner, regardless of TE material. In addition, set voltages less than +/-1 V and reset voltages on the order of +/-500 mV were observed with average R_{OFF}/R_{ON} ratios of 10^8. Examples of IV switching behavior for HfO_x-based devices are shown in Figure 6, below. Although this figure shows data from two different devices (one with a Ni TE and one with an Al TE) both unipolar and bipolar switching were observed for both of these TE materials.

Unipolar, bipolar and non-polar switching behavior have all been observed for HfO_x-based devices [9-10]. Similar to the TiO_x results (above), this could potentially be due to the Cu BE used in this study. Cu may well play a role in the switching behavior that is observed for some of these devices and other work by our group has shown that Cu may diffuse to the upper surface of the HfO_x during the deposition process [13]. This could have significant influence on the switching behavior of these devices.

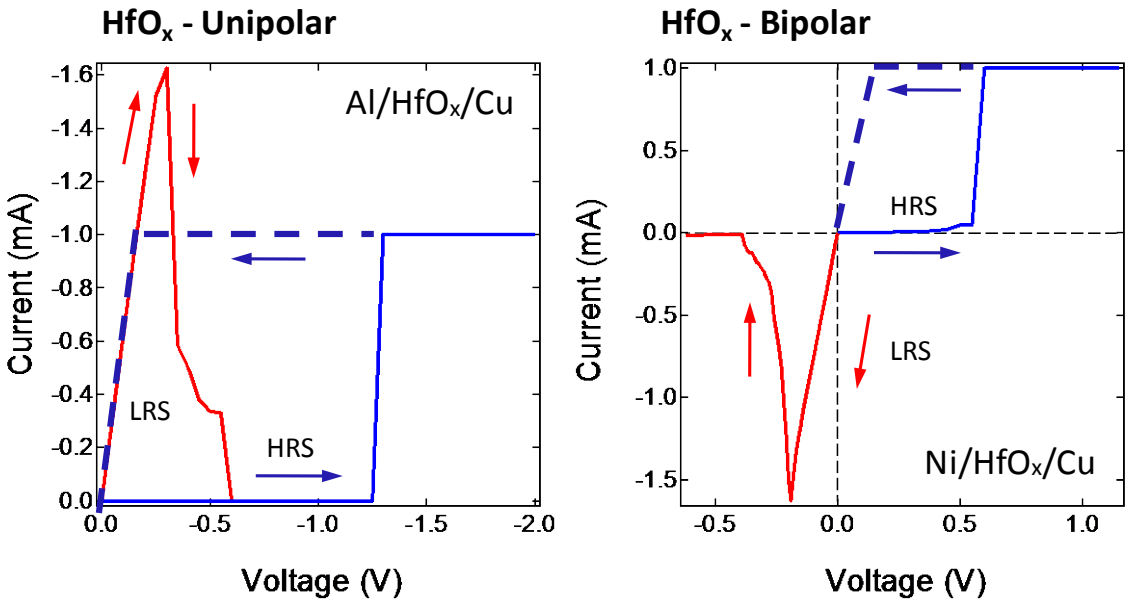


Figure 6: Current-voltage plots showing both unipolar (left) and bipoar (right) switching behavior for HfO_x devices. Switching behavior for HfO_x devices was independent of electrode material.

Cu_2O device behavior was strongly dependent upon TE material, and these devices did not demonstrate resistive switching behavior with either Au or Ni TEs. Further, only "mesa" devices exhibited consistent switching behavior. Devices that contained a continuous thermal oxide layer showed diode behavior independent of the top electrode. Mesa devices fabricated with Pt and Al TEs exhibited only bipolar switching behavior and repeated attempts at unipolar switching were unsuccessful. Current-voltage characterization indicated that the Cu_2O devices with Al TEs switch more consistently (at similar set and reset voltages) than those fabricated with Pt TEs. For the Cu_2O devices with an Al TE, set voltages ranged from 1.5-2.5 V, and reset voltages were less than -1V. The R_{OFF}/R_{ON} ratio for these devices ranged from 10^3-10^4. An example IV curve is shown in Figure 7 (below) for a Cu_2 device with an Al TE.

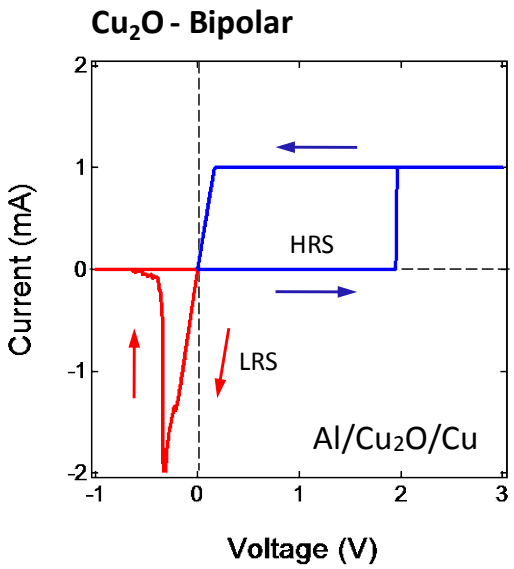


Figure 7: Current-voltage plot showing bipolar resistive switching behavior of Cu_2O based devices with Al top electrodes and Cu bottom electrodes.

In summary, devices with three types of metal oxides (Cu_2O, HfO_x, and TiO_x) demonstrated resistive switching characteristics which were highly dependent upon the type of material used for the TE. The results from this study are compiled in Table 1, below. This work shows that TE selection is an important factor for determining the resistive switching properties of MIM devices, and that this factor alone can determine switching polarity. Notably, not all TE / metal oxide combinations yielded switchable devices. Our work did not examine the role of the BE, since all devices tested used Cu BEs. Ongoing efforts in our group are focused on determining the role of BE on resistive switching characteristics, since this electrode could also have an important role in determining other aspects of switching behavior, including the set/reset voltage and R_{OFF}/R_{ON}.

Table 1. Summary of results from the metal oxide/top electrode survey.

Oxide	Synthesis	Top Electrode			
		Al	Au	Ni	Pt
Cu_xO	Thermal Oxidation	Bipolar	Diode	Diode	Bipolar
TiO_x	PVD (Ar)	Unipolar	Unipolar	Bipolar	Bipolar
	PVD (Ar and O_2)	Diode	Unipolar	Diode	Bipolar
HfO_x	ALD	Non-polar			

Conclusion from Metal Oxide Materials Screening:

Both the metal oxide insulator and the metal TE (independently) impact the resistive switching properties, in particular the switching polarity.

4.3.2 Evaluating the influence of copper on device properties

Rationale:

Hafnium oxide has been previously studied as the active layer in resistive memory devices by multiple groups. These investigations have demonstrated devices with stable, long-term read/write endurance [14-16], low switching energy [17], and high on/off ratios [15]. Previous work has shown the effects of Cu on the performance of HfO_x based resistive memory, by the insertion of a Cu layer between the HfO_x used to intentionally dope the HfO_x [15] or using Cu as a top electrode as a reservoir of metallic ions, thought to form conductive filaments during switching [16]. One principal result from the proceeding oxide-electrode study was the nonpolar switching behavior of the HfO_x devices. As copper is a mobile atom in this oxide material and is the *de facto* bottom electrode in this research, the role of copper doping on the switching properties of HfO_2 films created by atomic layer deposition was investigated.

Results:

The XPS depth profile of an as-deposited HfO_x film is shown in Figure 8 (a). There are three noteworthy points from these data. First, the profile shows that the HfO_x is not stoichiometric because the [O]/[Hf] ratio is equal to 1.1. Second, there is a significant (unintentional) copper impurity concentration present in the HfO_x. The latter is on the order of five atomic percent throughout the portion of the HfO_x layer that was analyzed. Even more surprising is the increase in the copper concentration at the beginning of the profile. The copper concentration in this region varies from a maximum of 60%, to 32% at the sample surface. Concurrently, the oxygen profile varies before stabilizing at 50% in the HfO_x layer. These data clearly indicate the final point; a copper oxide layer of varying stoichiometry resides on the surface of the HfO_x. The presence of this Cu_xO layer has not been reported previously. In addition, this layer could play a significant role in the electrical properties of these devices because Cu_xO has also been shown to be a resistive memory material [18].

Because it has better depth resolution and sensitivity to trace concentrations than XPS, SIMS was also employed to characterize the copper within the HfO_x. Figure 8 (b) shows the results from a SIMS analysis of a $Pt/HfO_x/Cu$ device structure. This device was profiled "as fabricated" and was therefore not influenced by any electrical bias before analysis. At the uppermost interface (Pt/HfO_x) the Cu signal peaks, along with O, indicating the presence of the Cu_xO layer. The estimated thickness of the Cu_xO is less than 20 nm. The accuracy of this thickness measurement from SIMS is limited by the differential sputtering rates of the materials in the MIM device structure. After the peak concentration of Cu at the interface, the concentration declines continuously, until another spike in Cu is observed at the beginning of the bulk Cu electrode. This is not an expected result. Normally, in a bulk diffusion process, we

would expect a decreasing concentration of Cu from the bulk bottom electrode to the surface, the opposite of what is observed. Further investigation is therefore needed to understand the profile of Cu observed in these structures as well as the trace concentration of Pt observed throughout the HfO_x region. Subsequent X-ray diffraction studies (not shown) indicated that the bulk structure of the film is amorphous, although this does not preclude regions of nanocrystallinity.

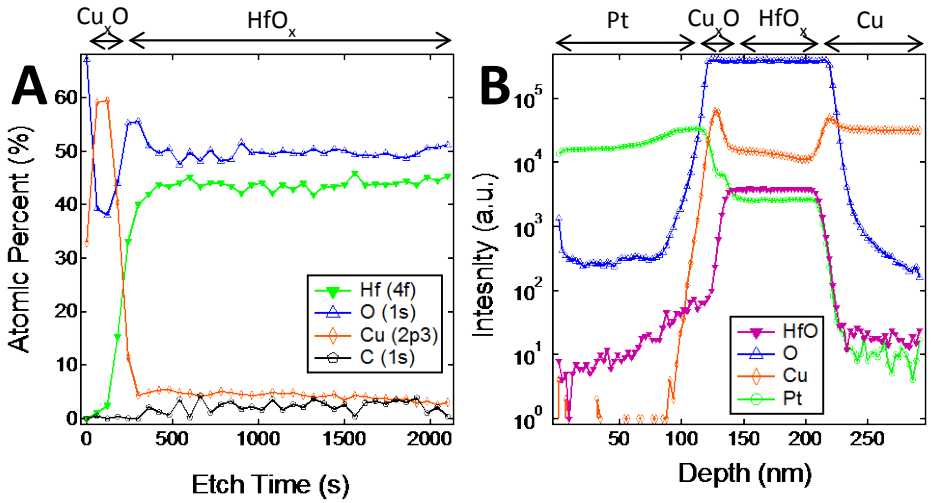


Figure 8: (a) XPS depth profile of ALD HfO_x on Cu. The uppermost portion of the profile shows Cu_xO layer formation. (b) SIMS depth profile of a Pt/HfO_x/Cu MIM device, confirming the presence of an interfacial Cu_xO layer.

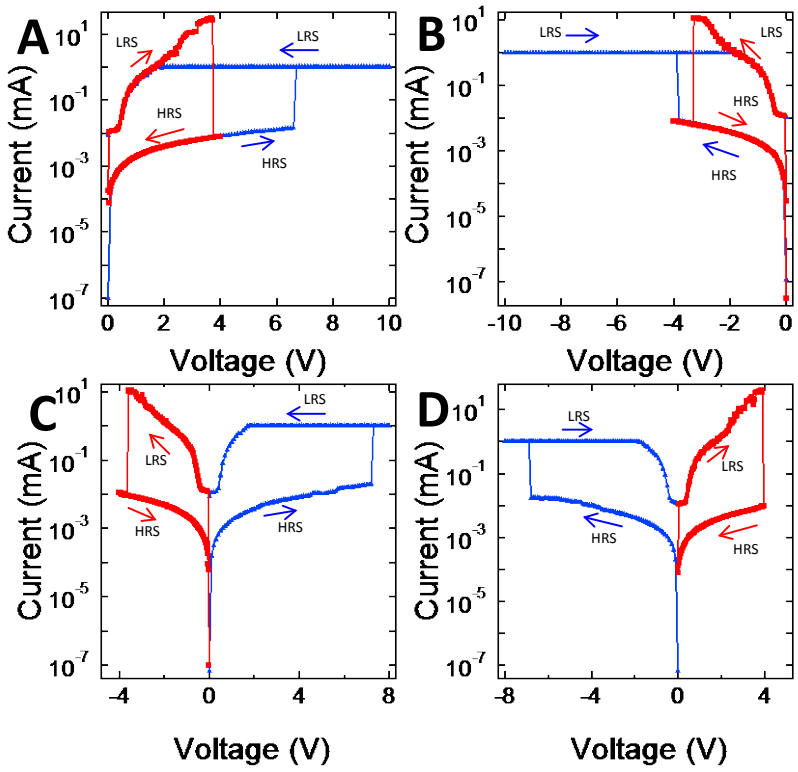


Figure 9: Current voltage measurements of a Pt/HfO_x/Cu MIM. (a)-(b) Unipolar operation, independent of bias direction. (c)-(d) Bipolar operation, with set voltage in both positive and negative polarity.

Top electrode biased current voltage measurements show both unipolar Figure 9 (a)-(b) and bipolar Figure 9 (c)-(d) resistive switching behavior. This behavior is known as "non-polar" resistive switching, in which only the magnitude of the voltage, not the polarity, dictates switching. The device in Figure 9. exhibited a change in resistance state during the application of a voltage sweep $[0 \rightarrow V_{set}]$ with V_{set} = |6-8| V. (Note: all sets used a 1 mA current compliance which was found to be the optimal value for these devices). Transitions from a LRS to HRS were where observed with a follow-up voltage sweep $[0 \rightarrow V_{reset}]$ of either polarity, with no current compliance. V_{reset} was consistent during each cycle at around |4| V. Previous studies report that HfO_x can behave as a unipolar [17], bipolar [16] or non-polar [14-15] switch. To the best of the author's knowledge, this is the first report of ALD HfO_x on Cu for resistive memory. Our process shows a significant, 5% Cu doping, very similar to the work of Wang *et al.*[15], who used a similar Cu doped HfO_x MIM (Cu/HfO_x/Cu/HfO_x/Pt) structure where a thin Cu layer was deposited between the HfO_x to dope it, in an attempt to improve switching performance. This group attributed the non-polar switching phenomena to the formation of Cu rich filaments, which form a low resistance conduction pathway. Our results of non-polar switching behavior agree very closely with the work of Wang *et al.* [15]. The unintended formation of the Cu_xO layer by ALD, does not appear to influence the root electronic mechanism, whether it be filamentary in nature, or an undiscovered phenomenon causing the non-polar resistive switching in HfO_x.

Devices exhibited sweep mode endurance of around 2-15 cycles before failure (as shorts). This is likely due to the large quantity of power applied to the device during sweep mode measurements. To alleviate this stress we employed pulse based measurements for the set operation. Figure 10 (a) shows the reset sweep measurements for multiple cycles after a pulsed set (pulse width of 10 µs with a pulse height of 3 V). There is no current measured for the first -0.7 V of the reset curve, due to the bias scheme of the device in the 1T1R configuration (Figure 10 (b)). In this configuration, a critical field is needed to overcome the drain to well junction barrier. Pulse based sets greatly improved the endurance of the devices (>30 cycles), and future work will include a complete set and reset pulsing study.

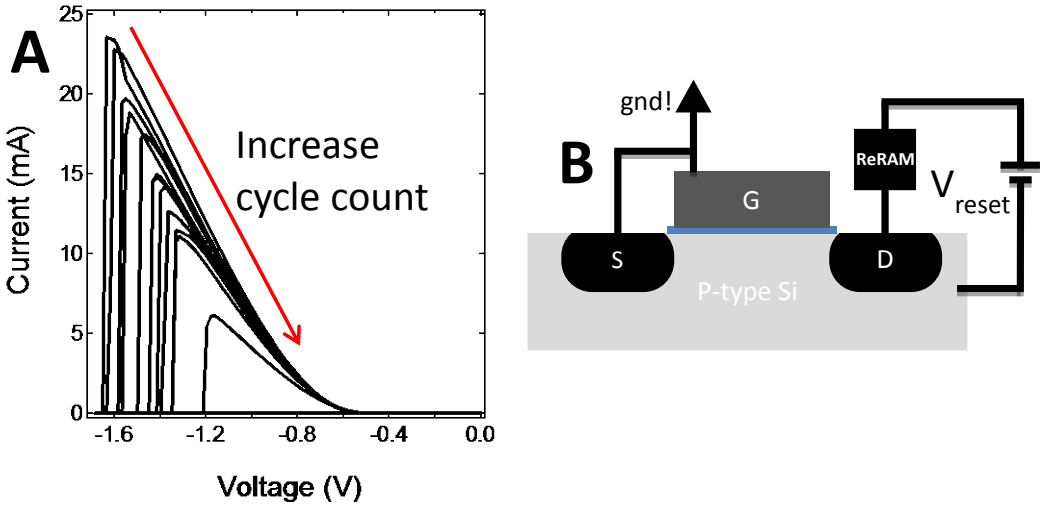


Figure 10: (a) Sweep mode I-V for reset, of a Ni/HfO_x/Cu MIM. Set operation carried out by application of pulse. (b) 1T1R configuration for reset I-V sweep.

Characterization of the nanoscale, via-based devices is shown in the focused ion beam milled, scanning electron microscopy (FIB-SEM) micrograph in Figure 11 (a). This image depicts a 200 nm Cu via array on a blanket Cu bottom electrode with 30 nm of ALD HfO_x. The depletion of Cu at the surface of the vias is likely occurring due to the same phenomenon which caused formation of Cu_xO on the HfO_x surface, as described above. Future work will determine if Cu_xO is also present at the surface, post ALD of HfO_x.

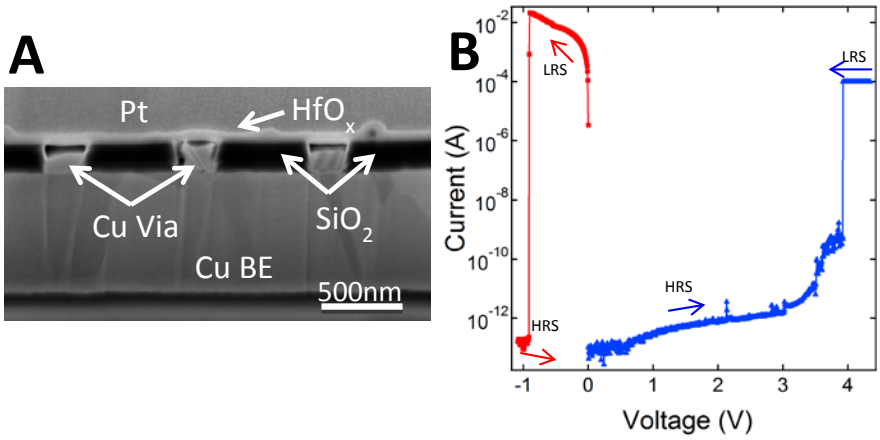


Figure 11: (a) FIB-SEM micrograph of 200nm Cu vias post ALD of HfO_x. Note Cu depletion at the surface of the Cu-filled vias. (b) Bipolar I-V of a 70nm Ni/HfO_x/Cu via device.

Sweep mode electrical measurements of the via based devices were performed in the same setup as the bulk film devices. Log plots of the I-V curves for a 70nm via are shown in Figure 11 (b), indicating bipolar behavior. V_{set} was below 5 V with a 100 µA current compliance (used to limit the total current density through the 70nm via). V_{reset} was less than 1 V, which yielded high I_{on}/I_{off} ratios of 10^{10} for these nanoscale devices.

Conclusions from evaluating the copper influence studies:

XPS and SIMS depth profiles showed that a ~20nm thick Cu_xO layer formed at the surface of the HfO_x. I-V data show non-polar resistive switching properties independent of top electrode material. Use of pulse mode measurement in a 1T1R configuration greatly improved endurance, by reducing total power dissipation stress during the set operation. Preliminary work on nanoscale via-based devices show bipolar switching characteristics with high I_{on}/I_{off} of 10^{10}. SEM images indicate, however, a large amount of Cu depletion at the surface of the via, due to the ALD of HfO_x. The influence of the copper depletion on crossbar fabrication/switching properties will be addressed later in section 4.4.

4.3.3 Alternative metal oxide fabrication methods development

Rationale:

Copper oxide is one of the transition metal oxides that exhibits resistance-based memory. Copper oxide RMDs have been produced with R_{OFF}/R_{ON} ratios up to 10^5 [19] and endurance values of $>10^4$ write/erase cycles [19]. Data retention times of >10 years have also been predicted [20-21]. Owing to copper's ubiquitous use as an IC interconnect metal, fabricating an

oxide from this material is very advantageous for resistive memory applications. In this work, a systematic investigation has been performed to determine how the oxide synthesis technique, film properties, and the device fabrication process impact the switching behavior of RMDs. Note that a novel oxygen implantation-based synthesis technique was invented as a part of this research. The latter is a patent in-progress. The results are not described in section 4.3.3 because they are described in detail in the attached manuscript (see Appendix) recently accepted for publication in *Applied Physics Letters*.

Results:

Copper oxide thin films produced by thermal oxidation over the temperature range 200-400°C exhibited rough surfaces. Figure 12 (a) shows the AFM height image of a copper oxide films synthesized at 300°C for 60 min. The RMS (root-mean-square) roughness of the image is 32 nm. The topography of the surface is evident from the 100 nm height scale of the image. Cuprous Oxide (Cu_2O) was the primary phase for all of the films produced by thermal oxidation; their XRD patterns were similar to Figure 15 (a) below. The majority of the devices fabricated from thermally oxidized copper exhibited a diode-like behavior as shown in Figure 12 (b). The diode-like behavior was observed in as-fabricated devices and after a large increase in current, similar to the set process common to RMDs. The diode behavior did not change with time or bias conditions and thus multiple resistance states were not observed for these devices. The diode- like IV behavior occurred independent of the top electrode used. Some devices fabricated from thermally oxidized copper with large area contacts (1 mm in diameter) exhibited bipolar witching; however, the resistance ratio (R_{OFF}/R_{ON}) was low (~1.5). The latter is due presumably to the large area of the contacts giving rise to low off-state resistance values.

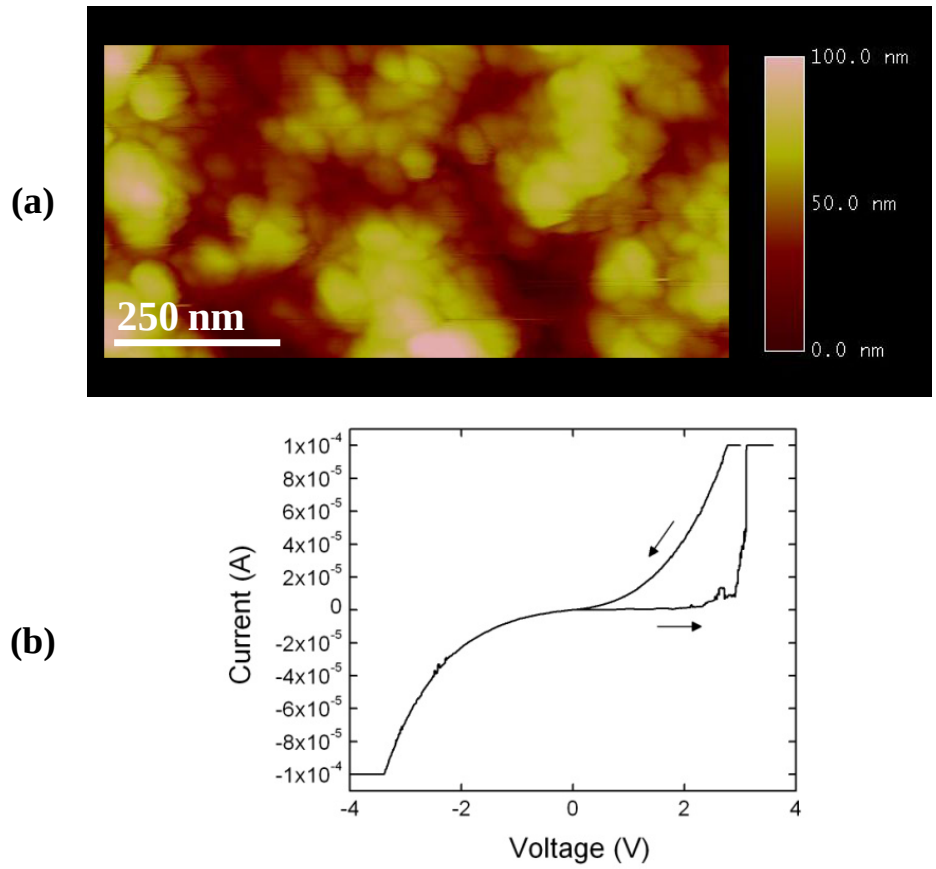


Figure 12: (a) AFM height image of the surface of thermally oxidized copper (300°C and 60 min.) and (b) the diode-like current-voltage behavior from a device fabricated from the same sample with an Al top electrode (100 nm).

Plasma oxidation of copper was also investigated as a route to synthesize copper oxide. Our results show that temperature plays a significant role in the oxidation rate and the microstructure in the resulting film. Plasma oxidation at room temperature yielded continuous thin films ranging in thickness from 5-10 nm, independent of the other process conditions. Figure 13 (a) shows a TEM image of a ~9 nm layer of copper oxide. Bipolar switching behavior was observed for devices fabricated from copper oxide synthesized by room temperature plasma oxidation. Figure 13 (b) shows the low resistance (LRS) and high resistance states (HRS) of a Al/Cu_xO/Cu device. The set voltage and the reset voltage were 2.8 V and -0.3 V, respectively, and the $R_{OFF}/R_{ON} = 10^8$.

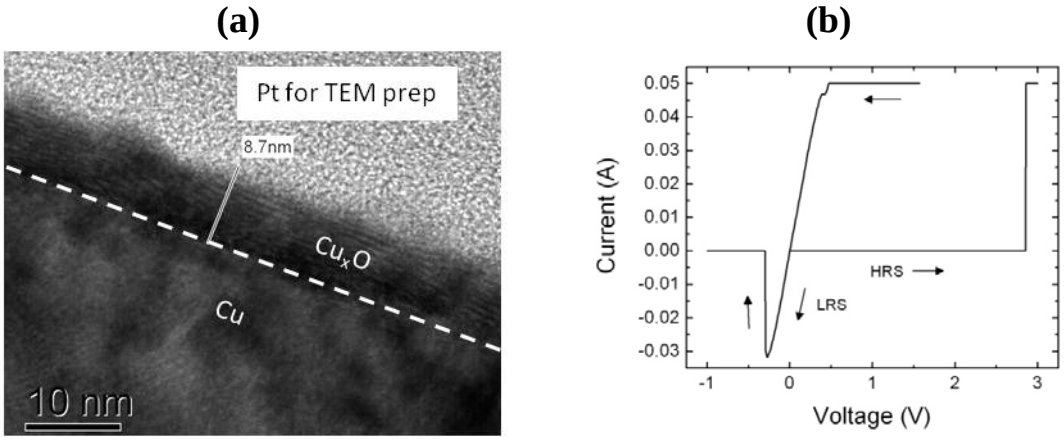


Figure 13: (a) TEM cross-sectional image showing a continuous thin film of RT plasma oxidized copper (300 Watts, 14 slm, 0.5 Torr, and 20 min.). (b) The bipolar switching behavior from a device fabricated from the same wafer with an Al top electrode (100 nm).

The copper oxide films produced by plasma oxidation at 280°C were significantly thicker than those created at room temperature. Figure 14 (a) shows a TEM image of a copper oxide film (>700 nm thick) that was created by high temperature plasma oxidation. Although it is not immediately apparent from Figure 14 (a), the thickness of these films varied dramatically (>10% thickness uniformity was observed), resulting in significant surface roughness/topography. Devices fabricated from the high temperature plasma oxide exhibited the same diode behavior described above and shown in Figure 12 (b).

Voiding at the copper-copper oxide interface was observed in films produced by thermal and plasma oxidation at temperatures ≥200°C. These defects are immediately apparent in Figure 14 (a); voids up to 200 nm in width separate the copper and the plasma oxide. Figure 14 (b) also shows a high degree of interfacial voiding in the cross section of a thermal oxide. Interfacial voids are clearly a problem for RMDs because they influence carrier transport between copper and copper oxide and thereby increase the resistance of the device. It is a noteworthy observation that the oxides that exhibit interfacial voiding also show the diode IV behavior. The latter is still being investigated. Other researchers have shown these defects are a common problem associated with copper oxidation and interfacial voids can form, for example, in areas with high impurity concentrations [22]. We are also investigating the origin of interfacial voiding in our process because these defects become more significant when scaling devices to smaller dimensions (see below).

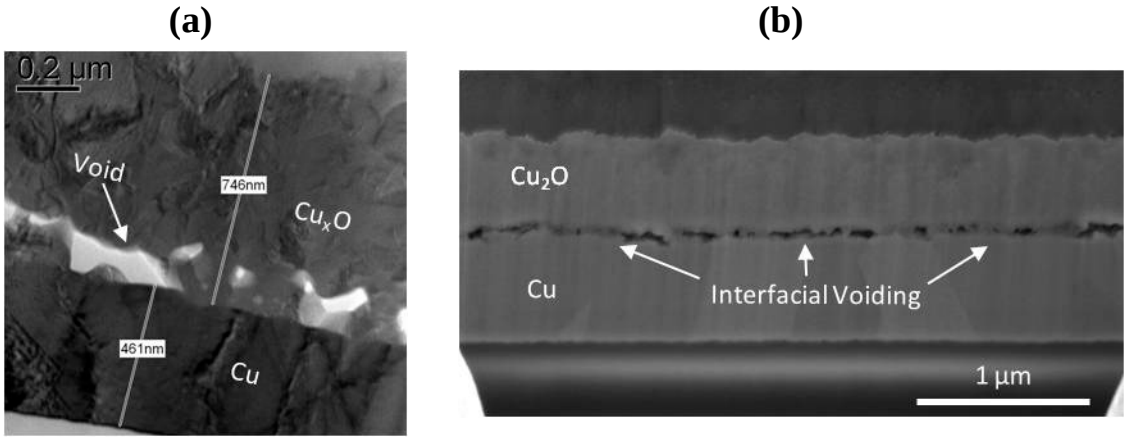


Figure 14: Voiding at the interface between copper and copper oxide synthesized by (a) plasma oxidation at 280°C (1000 Watts, 1 slm, 2.5 Torr, and 30 min.) and (b) thermal oxidation (300°C and 60 min.)

The copper oxide deposited by reactive sputtering had a polycrystalline microstructure with Cu_2O being the dominant phase present in the thin films. A representative XRD pattern for these films is shown in Figure 15 (a). The distinguishing feature of copper oxide synthesized by reactive sputtering over the oxides synthesized by oxidation was the large areas of open volume in the microstructure. As shown in Figure 15 (b), these areas were sufficiently large to permit electrical contact between the top and bottom electrodes. The latter lead to short circuiting (inset in Figure 15 (b)) in the devices fabricated from these films.

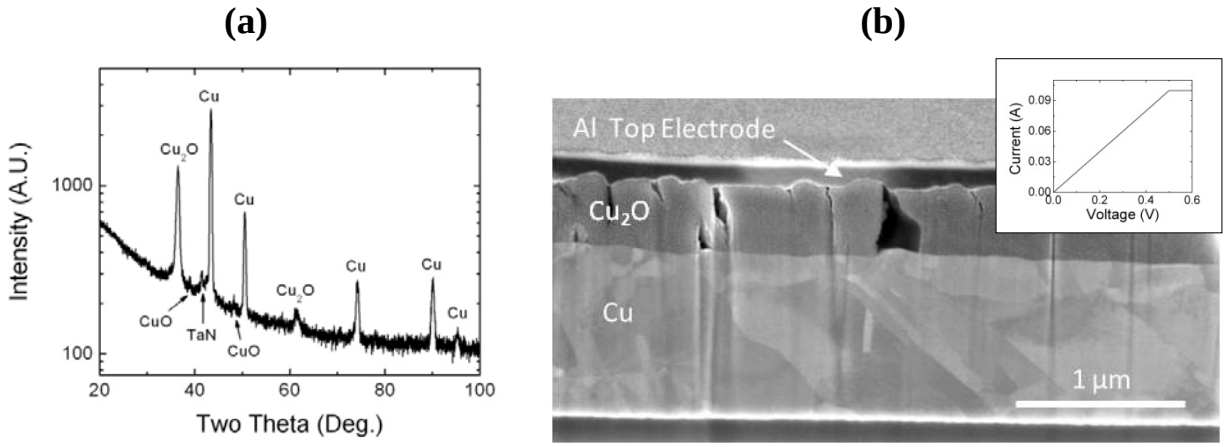


Figure 15: (a) XRD pattern showing Cu_2O is the primary phase in a copper oxide thin film deposited by reactive sputtering (Ar flow = 6.7 sccm). (b) SEM image showing the open volume in the copper oxide microstructure. This open volume allowed the top and bottom electrodes to make electrical contact, resulting in shorted devices (IV data inset).

A mesa etch process was developed to create isolated devices and prevent parasitic effects between individual devices. Of the chemistries suggested in ref. [23], phosphoric acid

gave the highest degree of selectivity, where the copper oxide layer between top electrodes was removed and the amount of undercutting below the top electrode was minimized. Figure 16 (a) shows a 100 µm device from the top and side (inset). The current-voltage characteristics of devices consisting of a continuous thermal copper oxide layer were compared with those that had been fabricated into individually defined mesa devices. Our preliminary results suggest that individually-defined mesa devices exhibit more reliable resistive switching characteristics. Figure 16 (b) shows the switching behavior for a thermal oxide mesa device. These data are markedly better than the diode behavior and the low resistance bipolar switching data discussed above for the continuous thermal oxide devices. Bipolar resistive switching was observed for mesa devices with both aluminum and platinum top electrodes. Nickel top electrodes were not utilized in the mesa device studies. Mesa devices with aluminum as the top electrode exhibited lower set voltages (<2.5 V) and higher R_{OFF}/R_{ON} ratios (10^3-10^4). The reset voltages were less than -1V for both Al and Pt top electrodes. We speculate that the improved switching properties of the mesa devices in this research are related to the increased current confinement in these devices over those with a continuous oxide layer. To improve the selectivity of the etch process and minimize the roughness shown in the inset in Figure 16 (a), a dry etch process is being developed similar to the work of Takano *et al.* [24].

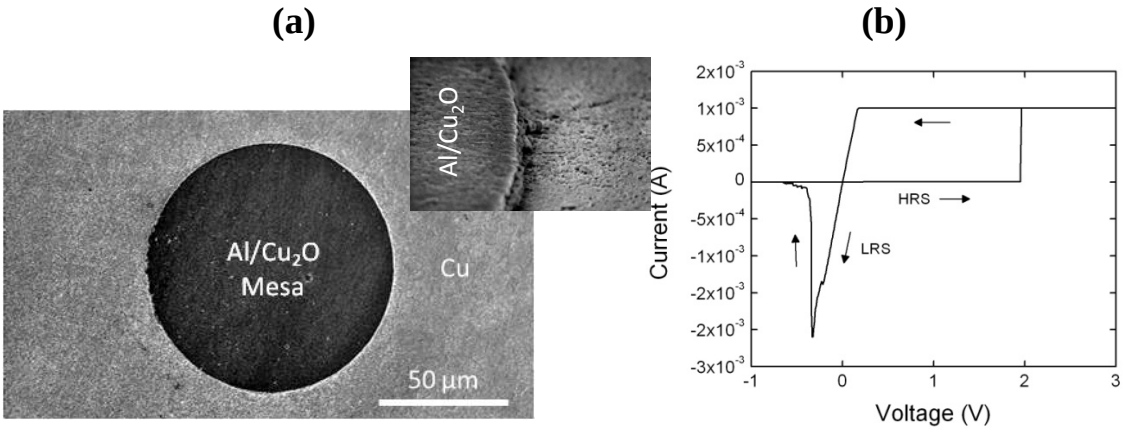


Figure 16: (a) Planview SEM image of a 100 µm (diameter) mesa device. The side profile is shown in the inset. The bipolar switching behavior for a mesa device on the same wafer is shown in (b); the top electrode was Al (100 nm).

There is a significant lack of information available in the open literature on the fabrication of nanoscale RMDs. The results of our preliminary work on synthesizing copper oxide into nanometer scale features is summarized here. Thermal oxidation of copper-filled vias created copper oxide in localized areas down to 33 nm in diameter; however the copper oxide separated from the underlying copper. Figure 17 (a) shows a cross-sectional SEM image of ~250 nm vias that have been oxidized at 300°C for 20 min. The gap between the copper oxide and the copper remaining in the via is likely the result of copper being depleted from this region during

oxidation and/or delamination induced by the lattice and thermal expansion mismatch between the materials. Copper oxide was also deposited into via structures by reactive sputtering. A representative SEM image of the wafer surface is shown in Figure 17 (b). The incomplete fill is clear. It is unclear if the large cracks in the surface of the copper oxide occurred during deposition or are a result of the post-deposition CMP step.

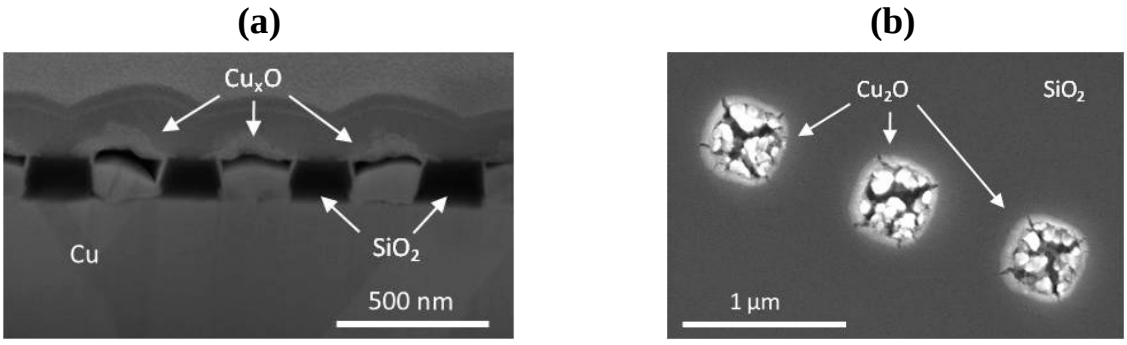


Figure17: SEM images showing: (a) the voiding between copper oxide and the copper remaining in 250 nm vias after thermal oxidation (300°C and 20 min.) and (b) 500 nm vias (post-CMP) that are partially filled with sputtered deposited (Ar = 20 sccm) copper oxide. The layers above the Cu_xO in (a) are protective Pt films from the FIB sample preparation.

Conclusions from alternative metal oxide fabrication study:

Copper oxide has been synthesized by thermal and plasma oxidation and reactive sputtering. Devices fabricated 1) from thin copper oxide layers and 2) into confined areas yielded the most robust switching characteristics. High oxidation rates produced copper oxide films with a defective microstructure. Voids at the copper-copper oxide interface made devices based on these films unsuitable for resistive memory applications. Further, interfacial voiding becomes much more significant as the device size decreases. This study has illustrated some of the challenges that will be encountered as copper oxide RMDs are scaled to smaller dimensions and integrated with CMOS. See the attached paper in the Appendix that details the properties of scaled copper oxide devices down to 48 nm that were created by oxygen implantation.

4.4 Fabrication and testing of a prototype 2 x 2 memristive crossbar logic element

4.4.1 Fabrication of crossbar devices

The first generation prototype 2 x 2 memristive crossbar was designed utilizing the copper via-based 300mm process flow described above. As shown in Figure 18, Cu vias extend vertically from the first metal layer (M1), labeled ECD Cu, to form the bottom electrodes within a glass TEOS insulating layer. 30 nm of HfO_x was then deposited across the wafer via atomic layer deposition through collaboration with Dr. Kevin Leedy of WPAFB. Removal of the blanket HfO_x from the surface of the probe pads was necessary to allow for electrical contact. To accomplish this, a separate optical lithography step and reactive ion etch was employed to selectively remove the HfO_x from the probe pad surface. Finally, electron beam lithography was used to define the top electrode pattern. The pattern was metalized in Ni using electron beam evaporation and then completed using a lift off technique. A completed single memristor and 2 x 2 crossbar imaged via SEM is shown in Figure 19.

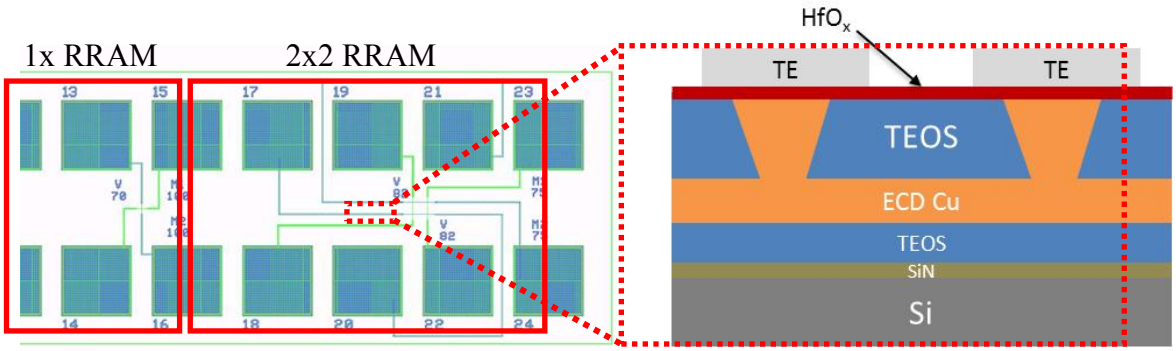


Figure 18: Left, Layout of the first generation crossbar design. Right, cross-sectional process of 2x2 crossbar.

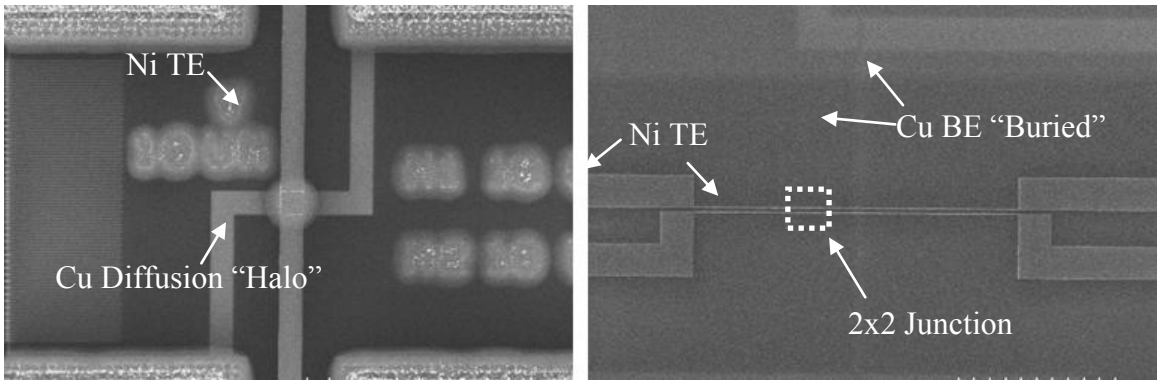


Figure 19: Left, SEM of a single memristive device. Right, SEM of 2x2 crossbar.

Several problems with the first generation design were discovered after fabrication was completed. Figure 20 shows a TEM cross section of a series of M1 lines contacted by a via. There is significant delamination of the Cu via from the side wall of the surrounding insulator as

well as large dishing of the insulator surface from CMP, causing the Cu vias to appear above the intended flush surface. The next issue involves the deposition conditions of the HfO_x. The HfO_x was deposited with a temperature of 250ºC, which was later discovered to cause diffusion of Cu through the HfO_x from the underlying via. This can be observed as a bright halo in the SEM image of Figure 19 (left) around the top and bottom electrode junction as well as in Figure 21 These problems with the first generation devices led to a redesign utilizing a new layout, modified process flow, and a different deposition technique for the HfO_x memristive layer.

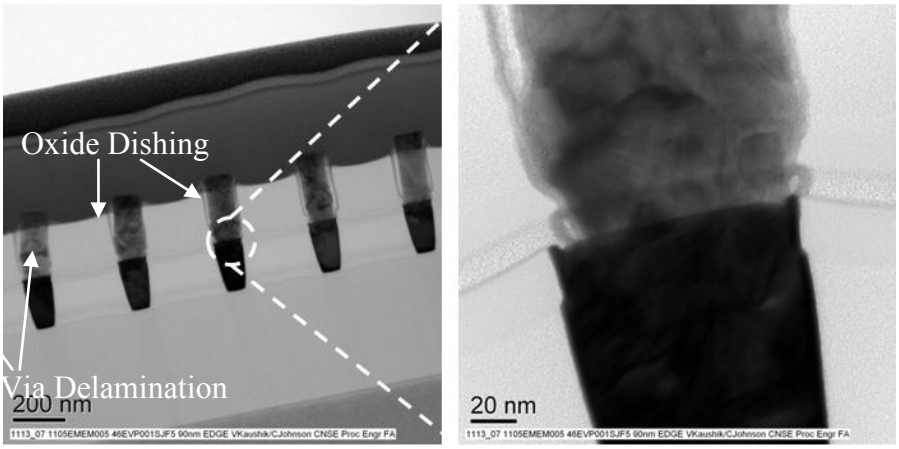


Figure 20: Cross -sectional TEM of Cu M1 contacted by a Cu via.

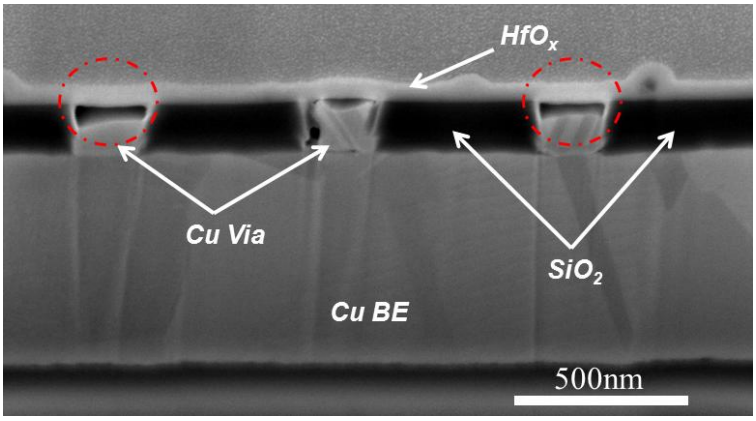


Figure 21: Cross sectional SEM of depleted Cu vias post-HfO_x by ALD. Open circuits shown in red circles, where limited conductivity and no change in resistance was observed.

The generation two crossbar has a new layout based on the "Raptor" mask set, which was designed for our follow-on memristor encryption projected sponsored by AFRL. The new layout shown in Figure 22 (left) simplifies the design allowing for shortened electrical connections and removes the stringent alignment tolerances imposed by the via design of the first generation process flow. The modified process flow is shown in Figure 22 (right). In this process, the HfO_x was deposited directly on top of the M1 Cu bottom electrodes and the lower contact via was removed from the build. Removal of the via solves the Cu adhesion and oxide dishing from the

first generation (Figure 20). The HfO_x deposition was also changed to a room temperature PVD process supplied by Canon-Anelva and the thickness was reduced from 50 nm to 15 nm. Figure 23 (left) shows a cross sectional TEM of a M1 Cu line covered by 15 nm of the new room temperature HfO_x. Pitting of the Cu surface was observed in the cross section of the smallest M1 lines 100 nm; this leads to pinholes in the blanket HfO_x. Top electrodes were fabricated using a new metal stack that consisted of Au/Ni/Ti. The thin Ti layer was introduced to act as an oxygen gettering layer [25]. Au was used to lower the top electrode line resistance and Ni served as a Au diffusion barrier. A cross sectional TEM image (Figure 23 (right)) shows a single node from a completed second generation 2 x 2 crossbar.

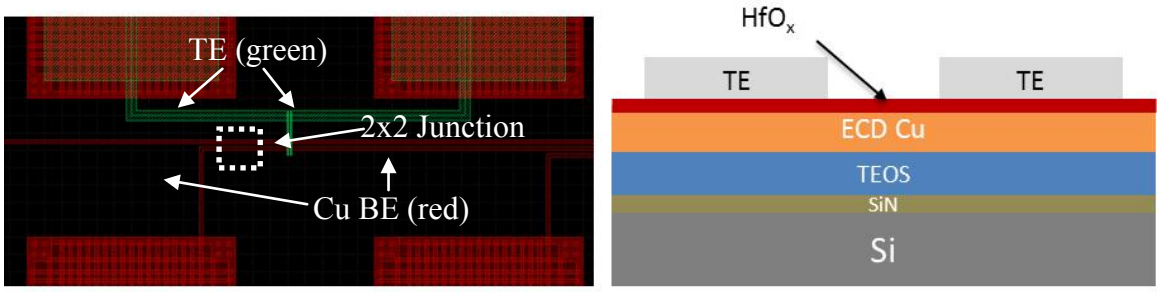


Figure 22: Left, Layout of second generation crossbar design. Right, Cross-sectional process of 2x2 crossbar; note the removal of the via layer.

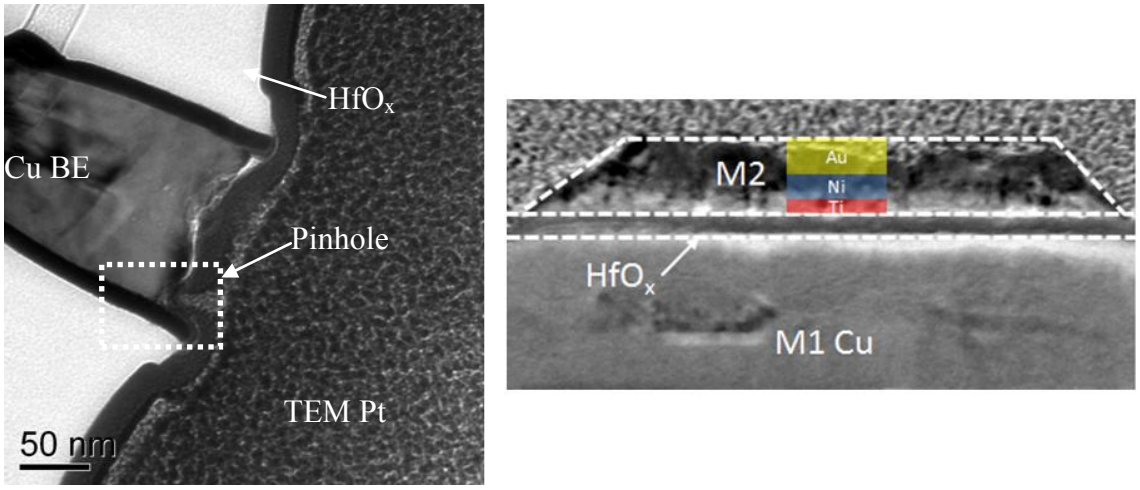


Figure 23: Left, TEM indicating pinhole formation in HfO_x. Right, TEM from a completed node of a 2x2 crossbar.

4.4.3 Evaluation of device performance

The second generation 2 x 2 crossbars were characterized using four simultaneous microprobes contacting each of the four pads of the crossbar. DC source-measure units from an Agilent semiconductor parameter analyzer were connect to each probe. Each node was tested individually by addressing the correct top and bottom electrodes for the corresponding node. After a switch was performed on a particular node, the other three nodes states were measured with a low voltage resistance read to detect any crosstalk that may have been occurring. A characteristic bipolar IV plot from a single node is shown in Figure 24, which shows ten overlapping set/reset sweeps. Devices were consistent with set voltages < 2.5 V and reset voltages < -0.5 V. Resistance ratios between the high resistance and low resistance states were ~10^2. ~10^3 switching cycles were observed from a 10 µm device fabricated using the generation two design (Figure 25). No crosstalk was observed during several cycles of each node. Due to the previously discussed pitting of the M1 Cu lines, the device yield was ~50%.

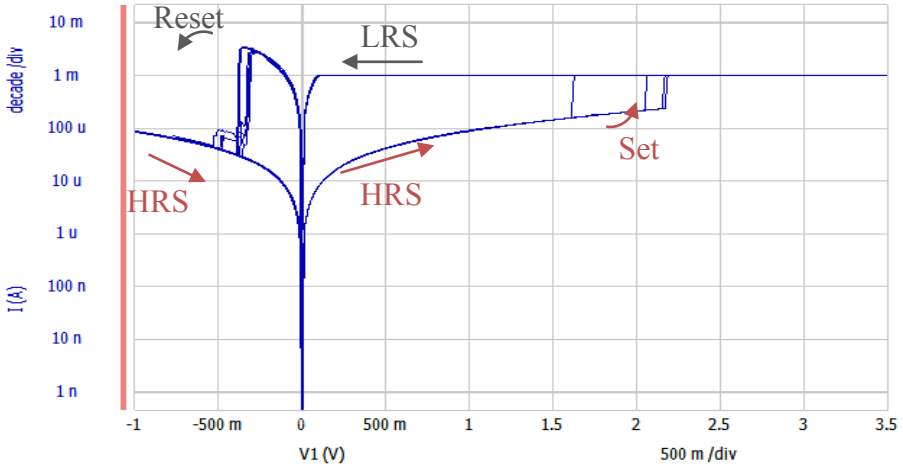


Figure 24: Characteristic bipolar switching plot from a single node of a 2x2 cross bar.

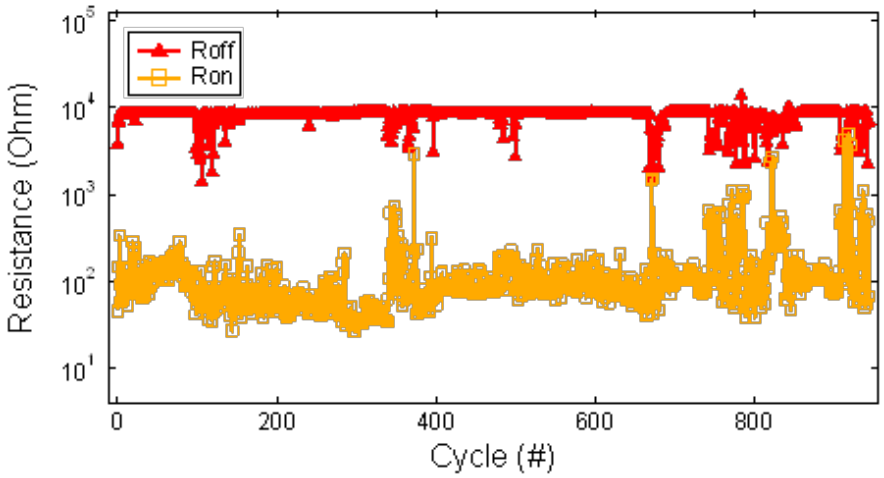


Figure 25: Switching endurance from a 10 µm memristor

A third generation of devices are being developed as part of the already mentioned encryption program. This new process will create defined regions of HfO_x specific to the device region, and utilize a Cu dual-damascene process for the top electrode contact and wiring. The third generation devices are based upon the Raptor maskset, which includes designs of scaled cross bar circuits ranging from 12 x 12 to 128 x 128 arrays that will allow us to study large memristive arrays. A preliminary cross section from a 12 x 12 array featuring the new Cu top electrodes and wiring is shown in Figure 26; this build does not include a HfO_x memristive layer, as this portion of the process is still under development.

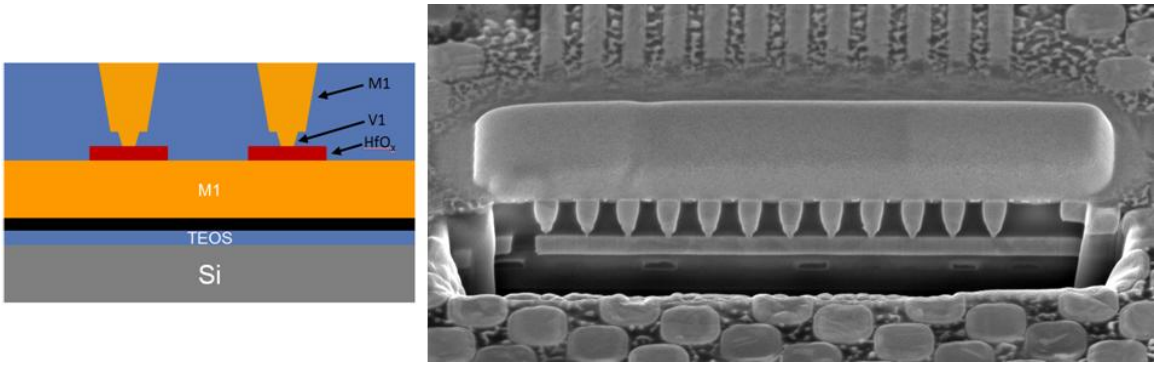


Figure 26: Left, proposed process from Gen3 Raptor memristive devices. Right, cross-sectional SEM of a 12 x 12 cross bar development (no HfO_x).

Conclusions/Summary from device fabrication and testing:

Multiple generations of 2 x2 crossbars have been fabricated and characterized. The first generation devices were designed around a damascene via approach, in which the copper filled via served as the bottom electrode. Issues during Cu plating and CMP caused voiding,

delamination and dishing within the vias. These issues negatively impacted the yield of the subsequently fabricated devices and ultimately hindered the viability of the first generation process. In addition, ALD of HfO_x at 250°C lead to large out-diffusion of Cu from the via into the overgrown HfO_x film, rendering the bottom electrode via in many cases non-conducting. A second generation design was implemented to resolve both the via and ALD HfO_x issues. The second generation devices again used Cu as the bottom electrode, but instead of using a terminated via, we used the surface of a M1 line, which greatly improved the robustness of the Cu bottom electrode. Room temperature PVD was used to deposit the HfO_x films and minimize the copper out-diffusion. Based on results reported in the scientific literature, top electrodes of Ti/Ni/Au were fabricated to improve switching characteristics and line resistance. Electrical performance of the second generation devices yielded high endurance (up to 10^3 cycles), stable memory windows (~10^2), and functional 2x2 crossbars with junction widths of 500 nm. Future work on a third generation of devices is currently underway, with plans to scale the cross-bar architecture and process flow to larger 12x12 and 128x128 arrays.

4.5 Presentations, Publications and Patent Applications in This Project Period

Presentations

1. S.M. Bishop, B.D. Briggs, K.D. Leedy, H. Bakhru, and N.C. Cady, "Properties and Challenges of Scaled Resistive Memory", International Semiconductor Device Research Symposium, Baltimore, MD, Dec. 2011.

2. N.R. McDonald, S.M. Bishop, B. D. Briggs, J. E. Van Nostrand, and N.C. Cady, "Analysis of Nonpolar Resistive Switching Exhibited by Al/Cu_xO/Cu Memristive Devices Created via Room Temperature Plasma Oxidation", International Semiconductor Device Research Symposium, Baltimore, MD, Dec. 2011.

3. B.D. Briggs, S.M. Bishop, J.O. Capulong, M.Q. Hovish, R.J. Matyi, and N.C. Cady, "Comparison of HfO_x-Based Resistive Memory Devices with Crystalline and Amorphous Active Layers", International Semiconductor Device Research Symposium, Baltimore, MD, Dec. 2011.

4. B.D. Briggs, S.M. Bishop, K.D. Leedy, T. Murray, K. Dunn, R. Matyi, J. Van Nostrand, and N.C. Cady, "Characterization of the Interfacial Cu_xO Layer in HfO_x/Cu Resistive Memory", Physical Electronics Conference, College of Nanoscale Sci./Eng., Univ. at Albany, Albany, NY, June 2011.

5. S.M. Bishop, B.D. Briggs, Z.P. Rice, S. Addepalli, N.R. McDonald, and N.C. Cady, "Challenges in the Fabrication of Copper Oxide Resistive Memory Devices", Spring MRS 2011, San Francisco, CA, April 2011.

6. B.D. Briggs, S.M. Bishop, K.D. Leedy, B. Butcher, R. L. Moore, S. W. Novak, and N.C. Cady, "Influence of Copper on the Switching Properties of Hafnium Oxide-Based Resistive Memory", Spring MRS 2011, San Francisco, CA, April 2011.

7. S.M. Bishop, B.D. Briggs, K.D. Leedy, S. Addepalli, and N.C. Cady, "A Survey of Metal Oxides and Top Electrodes for Resistive Memory Devices", Spring MRS 2011, San Francisco, CA, April 2011.

Conference Proceedings Articles

1. S.M. Bishop, B.D. Briggs, Z.P. Rice, S. Addepalli, N.R. McDonald, and N.C. Cady, "Fabrication and Characterization of Copper Oxide Resistive Memory Devices", *Mater. Res. Soc. Symp*. 1337 (2011) 55.

2. B.D. Briggs, S.M. Bishop, K.D. Leedy, B. Butcher, R. L. Moore, S. W. Novak, and N.C. Cady, "Influence of Copper on the Switching Properties of Hafnium Oxide-Based Resistive Memory", *Mater. Res. Soc. Symp.* 1337 (2011) 49.

3. S.M. Bishop, B.D. Briggs, K.D. Leedy, S. Addepalli, and N.C. Cady, "A Survey of Metal Oxides and Top Electrodes for Resistive Memory Devices", *Mater. Res. Soc. Symp*. 1337 (2011) 91.

Journal Articles

1. S.M. Bishop, H. Bakhru, S.W. Novak, B.D. Briggs, R.J. Matyi, and N.C. Cady "Ion Implantation Synthesized Copper Oxide-based Resistive Memory Devices" *Appl. Phys. Lett.* 99 (2011) 202102.

2. N. R. McDonald, S. M. Bishop, B. D. Briggs, J. E. Van Nostrand, and N.C. Cady "Analysis of Nonpolar Resistive Switching Exhibited by Al/Cu_xO/Cu Memristive Devices Created via Room Temperature Plasma Oxidation" Submitted to *Sol. State Elect.* (2011) In Review

Patent Applications

1. S. M. Bishop and N.C. Cady, "Ion Bombardment Synthesis of Transition Metal Oxide-Based Memory Devices", Filed on 8/23/2011 (Serial No. 61/526537).

5. Conclusions

This effort has resulted in crossbar resistive memory devices / memristors that can be used for future memory and logic applications. Multiple metal oxides were evaluated for integration into crossbar memristors, with hafnium oxide being the ideal candidate for future study, due to ease of integration, endurance, and performance parameters. Copper oxide is also a viable material, but fabrication and performance issues could make long-term integration of this material challenging. In addition to characterizing metal oxides deposited by thin film deposition methods, we also established a novel *in situ* fabrication method of converting metals to metal oxides. This oxygen ion beam modification method is the subject of the attached paper (Appendix 1) as well as a provisional US patent application filed during the course of this effort. This method is promising for scaled-up manufacturing of memristive devices.

The modeling and simulation efforts described in this report show that memristors in a 1T1R configuration have better performance characteristics than a simple one memristor configuration. This may have to do with current overshoot during the switching or forming steps of operation. Further, modeling shows that there may be intermediate switching states (partial switching) during pulse-mode operation. This will be explored further in subsequent efforts. Finally, we have fit some of our device data to literature-based physical models (see Appendix 1 and Appendix 2) which show that our devices behave similar to what is expected for "filament" based memristors. We hypothesize that our use of a copper bottom electrode may be influencing filamenet formation, possibly by introducing a metallic copper filament into the metal oxide dielectric. Future efforts will seek to identify these filaments and to engineer the materials system for increase switching endurance, which may be highly dependent upon these filaments.

Lastly, we have delivered a 2 x 2 crossbar device that shows resistive switching behavior (memristance). These devices will be expanded in subsequent efforts to larger arrays (12 x 12, 128 x 128) and the size of the individual crossbar elements will continue to be reduced (50 nm and smaller).

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List of Acronyms

RRAM: Resistive random access memory

ReRAM: Resistive random access memory

RMD: Resistive memory device

TE: Top eleectrode

BE: Bottom electrode

HRS: High resistance state

LRS: Low resistance state

XPS: X-ray photoelectron spectroscopy

XRD: X-ray diffraction

TEM: Transmission electron microscopy

Appendix 1. Applied Physics Letters Publication

APPLIED PHYSICS LETTERS 99, 202102 (2011)

Ion implantation synthesized copper oxide-based resistive memory devices

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Copper oxide resistive memory layers have been synthesized by ion implantation. Devices fabricated from off-stoichiometric Cu_2O exhibited unipolar switching in forward/reverse bias without a forming voltage. The on-state conduction of these devices is likely dominated by a metallic filament, which ruptures via Joule heating to transition the device to the high resistance off-state. Technology scaling was achieved by oxygen implanting copper filled vias. The resulting via-based memory devices exhibited unipolar resistive switching down to 48 nm in diameter. © *2011 American Institute of Physics*. [doi:10.1063/1.3662036]

Copper oxide is a transition metal oxide that exhibits memory resistance. Lv and co-workers have demonstrated copper oxide resistive memory devices (RMDs) with resistance ratios up to 10^5 (Ref. 1) and endurance of $>10^4$ cycles.[2] In addition, retention times >10 years have been extrapolated with critical temperatures $<100\,^{\circ}C$.[1,3]

One advantage copper oxide has over other resistive memory oxides is it can be synthesized in a fully back-end-of-line compatible manner. Chen *et al.*[4] have integrated copper oxide RMDs into a 64 kbit 1T-1R (one transistor-one resistor) configuration using thermally oxidized 180 nm copper filled vias. To meet industry scaling requirements, the minimum feature size must be reduced significantly using alternative strategies to thermal oxidation because voiding occurs at the oxide-via interface in sub-100 nm devices.[5]

Ion implantation is well-suited for synthesizing scaled memory oxide layers because of its extensive use in integrated circuit fabrication and the large defect concentrations created during high dose implantation. The latter is potentially advantageous because resistive switching is commonly linked to defects within the oxide layer.[6]

The starting 300 mm silicon wafer was coated with a SiO_2/SiN insulating layer followed by a Cu/Ta/TaN multilayer (seed layer/adhesion layer/diffusion barrier) for Cu electrodeposition (ECD). ECD was followed by chemical mechanical planarization (CMP), yielding polished 1 μm thick Cu films. Ion implantation was performed on cleaved samples with 5×10^{16}/cm^2 O^+ ions at energies of 30, 50, and 100 keV. Top electrodes were fabricated using shadow masks or conventional photolithography-based lift-off processing. The Al top electrodes were deposited to 100 nm by electron beam evaporation; the resulting contacts were approximately 100 μm × 100 μm.

X-ray photoelectron spectroscopy (XPS) was performed using a ThermoFisher Thetaprobe equipped with a hemispherical analyzer and a monochromated Al Kα x-ray source (1486.6 eV). X-ray diffraction (XRD) measurements were made with a Bruker D8 diffractometer with a graded parabolic mirror at the source, a parallel-beam geometry with Soller slits in the incident/diffracted beam paths and a fixed 0.5° angle of incidence. All current-voltage (I-V) measurements were performed with an Agilent B1500A parameter analyzer with the top electrode biased and the bottom electrode grounded.

The XPS depth profile of a copper film implanted with oxygen (5×10^{16}/cm^2 and 30 keV) is shown in Fig. 1(a). The O1s data reach a maximum at 11.9 at. % (~300 s) and subsequently decay to ~0 at. % (1500–2000 s). XRD measurements performed on the same film (Fig. 1(b)) show the oxide is polycrystalline as-implanted (i.e., without a post-implant anneal) and Cu_2O is the dominant oxide phase. While the Cu peaks were very close to their expected positions, the Cu_2O peaks were shifted to significantly higher angles, indicating a reduction in lattice parameter of $\Delta a/a \approx 2.1\%$. Based on the latter and that the peak concentration from XPS is significantly less than that expected for stoichiometric Cu_2O, we interpret the XRD data as evidence that the implant synthesized oxide is substoichiometric but still with sufficient crystalline perfection to produce the Bragg reflections for the Cu_2O phase of copper oxide.

Figure 2(a) shows the switching behavior from RMDs fabricated from copper oxide synthesized by ion implantation. Ion implantation was performed with three sequential 5×10^{16}/cm^2 O^+ doses at energies of 30, 50, and 100 keV, so the resulting depth profile would closely mimic the abrupt composition profile expected from other synthesis techniques. Unipolar switching behavior, in which SET and RESET occur in the same voltage polarity, was observed in forward/reverse bias. SET refers to the transition from the low resistance on-state (LRS) to the high resistance off-state (HRS), while RESET refers to the reverse transition. The SET voltage (V_{SET}) and RESET voltage (V_{RESET}) and current (I_{RESET}) are denoted in Fig. 2(a). The Ohmic ($I \propto V$) correlation in Fig. 2(b) suggests that LRS conduction is dominated by a metallic filament, as opposed to an ionic filament that exhibits linear and parabolic conduction.[7]

Devices A and B were tested in forward bias twenty and ten times, respectively, using a current compliance of 5-10 mA. The average V_{SET} (±standard deviation) was 2.23 V (±0.98 V) for Device A and 2.56 V (±0.52 V) for Device B. The V_{SET} was strongly dependent on the off-state resistance (R_{OFF}). While V_{SET} for both devices fell within 0.61–4.89 V, R_{OFF} ranged between 10^4 and 10^{14} Ω. Kim *et al.* have shown

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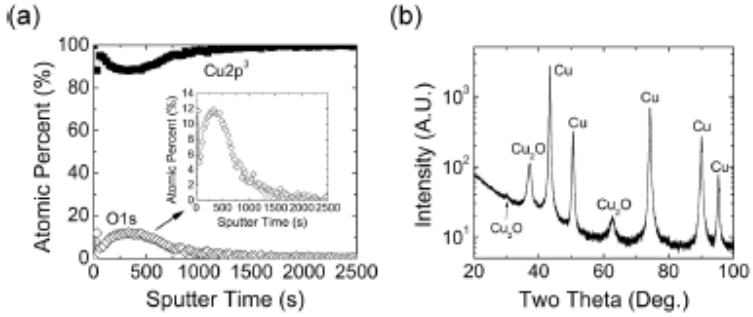

FIG. 1. (a) XPS depth profile and (b) XRD pattern of a copper thin film ion implanted with oxygen.

that similar data suggest space-charge-limited-conduction in the HRS.[8] In the LRS, R_{ON} ranged between 50 and ~2500 Ω. As a result, R_{OFF}/R_{ON} ranged from 8×10^2 to 8×10^{11}. For Device A and Device B, the average RESET voltages were 0.93 V (±0.58 V) and 0.61 V (±0.33 V), respectively.

Figure 3 shows that I_{RESET} is inversely proportional to the square root of R_{ON}. The significance of the power-law fits will be subsequently analyzed. The critical temperature (T_{CRIT}) for filament dissolution via Joule heating is related to the dissipated electrical power (P_{RESET}) and the equivalent thermal resistance of the filament (R_{TH}) by $T_{CRIT} = T_0 + P_{RESET}(R_{TH})$, where $T_0 = 300$ K.[9] Taking the electric power as $P_{RESET} = I_{RESET}^2(R_{ON})$ and solving for I_{RESET} gives

$$I_{RESET} = \sqrt{\frac{T_{CRIT} - 300}{R_{TH}}}(R_{ON})^{-1/2}. \quad (1)$$

From this equation, the relationships between I_{RESET} and R_{ON} (Device A: $y = 74.8x^{-0.53}$ and Device B: $y = 41.2x^{-0.471}$) are consistent with a RESET process based upon filament rupture caused by Joule heating. These data, in conjunction with the Ohmic ($I \propto V$) correlation in Fig. 2, further support the hypothesis that the LRS conduction mechanism is filamentary.

The proportionality constant from Eq. (1) can be related to the filament diameter (d) by taking the thermal resistance as $R_{TH} = l/(8\kappa_{eq}A)$.[9] A is the circular cross-sectional area, κ_{eq} is the equivalent thermal conductivity, and l is the filament length. The resulting equation is

$$\text{Constant} = \sqrt{\frac{T_{CRIT} - 300}{R_{TH}}} = \sqrt{\frac{T_{CRIT} - 300}{l/(2\kappa_{eq}\pi d^2)}}. \quad (2)$$

Taking the ratio of the proportionality constants for Device A and B from Fig. 3 and assuming the critical temperature and thermal conductivity are the same for A and B, the filament diameter for Device B (d_B) is approximately two times (Constant A/Constant B = $d_B/d_A = 1.8$) the filament diameter of Device A (d_A). This suggests that the difference in the reset behavior between A and B is related to the difference in the filament diameter.

The I-V data in this work support single filament mediated conduction in the LRS. Staircase-like resistance changes attributed to the formation of multiple filaments were not observed during SET.[10] The diameter of a filament can be estimated using $R_{ON} = \rho\frac{l}{A}$. From the bulk resistivity of Cu ($\rho_{Cu} = 1.67 \times 10^{-6}$ Ω cm),[11] the thickness of the implanted oxide ($l \approx 250$ nm), and the average R_{ON} from Fig. 2 ($R_{ON} = 2.6$ kΩ), the calculated diameter is 1.4 nm. It is likely this value is larger because ρ_{Cu} increases as feature size decreases.[12] Takagi and co-workers[13,14] have studied filaments within Cu_xO RMDs. Their work shows that switching behavior is controlled by a single copper filament within copper-rich copper oxide. Based on resistivity measurements, these authors speculate the copper filament is on the order of tens of nanometers, which is within range of the value above.

No forming voltage was needed to initiate the unipolar switching discussed above. Prior work has shown forming free copper oxide RMDs when the oxide layer was the Cu_2O phase and the layer thickness was decreased.[2,15] The lack of a forming voltage here is consistent since polycrystalline Cu_2O was the dominant phase post-implantation. Because the implantation-synthesized copper oxide layers in this work are substoichiometric, the forming-free resistive

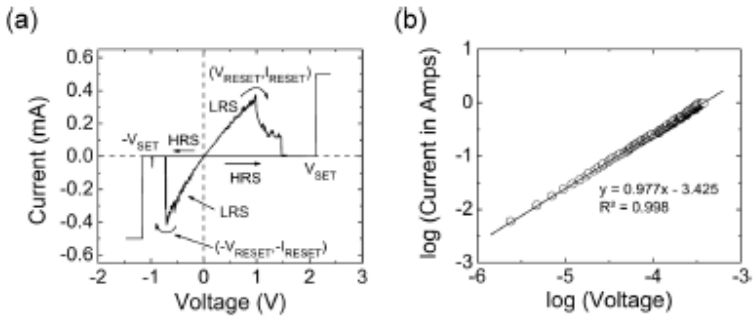

FIG. 2. (a) Typical unipolar switching behavior of a RMD fabricated from implantation-synthesized copper oxide. (b) Log-log plot of the LRS I-V data from the positive bias region of (a).

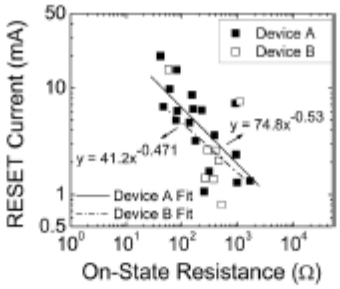

FIG. 3. Correlation between the RESET current (log scale) and the on-state resistance (log scale).

switching could be linked to vacancies within the copper oxide. Chen *et al.* have demonstrated forming-free switching driven by process-induced vacancy formation.[16] These investigators introduced vacancies by depleting oxygen from HfO_x using a titanium layer between the oxide and top electrode. It is reasonable to assume that vacancies exist within our devices from the implantation process and/or a similar oxygen depletion caused by the aluminum top electrode (which has been demonstrated previously[17]). Son and Shin have shown that defects at grain boundaries can serve as leakage current pathways in RMDs.[18] It is plausible that vacancies could exist at grain boundaries in our devices from either of these sources, providing parasitic current pathways and thus eliminating the need for a forming voltage.

The scalability of implantation synthesis was analyzed by oxygen implanting copper filled vias fabricated using a copper damascene process.[19] Ion implantation was performed with $5 \times 10^{16}/cm^2$ O^+ ions at 30 keV and aluminum top electrodes were fabricated as outlined above. This process yielded switchable devices from implanted vias down to 48 nm in diameter (Fig. 4). The SET voltage was −2.11 V, while the RESET voltage (current) was −0.52 V (−2.96 mA).

Ion implantation has been utilized to synthesize copper oxide resistive memory layers. XRD/XPS measurements

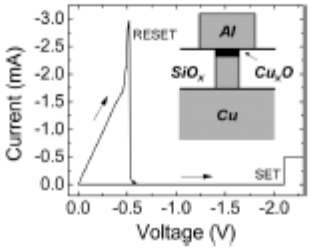

FIG. 4. Unipolar switching behavior for a 48 nm copper-filled via RMD.

suggest that a defective, sub-stoichiometric Cu_2O was produced. The defective nature of the film could play a significant role in the switching properties, in particular the forming voltage. The I-V data suggest that LRS conduction is dominated by a metallic filament and RESET is facilitated by filament rupture through localized Joule heating. The ability to scale the technology to 48 nm demonstrates the potential of this approach for nanoscale RMD fabrication.

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Appendix 2. Solid State Electronics Submitted Manuscript

Analysis of Nonpolar Resistive Switching Exhibited by Al/Cu_xO/Cu Memristive Devices Created Via Plasma Oxidation

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***Abstract*—In this study, Cu_xO was created via plasma oxidation under varying reactive ion etch (RIE) conditions, 100-300 W, to observe the affects upon subsequently fabricated Al/Cu_xO/Cu memristive device operating parameters. The resulting Cu_xO thin films ranged in thickness from 40-620 nm as determined by secondary ion mass spectrometry (SIMS) analysis. X-ray photoelectron spectroscopy (XPS) analysis also indicated that the Cu:O atomic ratios of these films increased from 1:1-3:2 with increasing RIE power. After applying Al top electrodes, the memristive devices demonstrated complete nonpolar switching with SET and RESET voltages of ± 2-3 V and ± 0.5 V, respectively. High to low resistance state ratios up to 4,000 were observed but decreased with increasing oxide thickness. The reset current was inversely proportional to the oxygen concentration within the copper oxide thin films. Both Ohmic and Poole-Frenkel effect conduction were observed in the high resistance state for devices that exhibited resistive switching. Only Ohmic conduction was observed in the low resistance state. Devices which did not switch also adhered to Poole-Frenkel effect conduction at high voltages. Based on these data, the switching mechanism of these devices is still not well understood.**

Keywords: Plasma oxidation, Cu_xO, memristive device, nonpolar

1. Introduction

There has been a marked rise in interest over the past several years in the area of memristive devices or restive RAM [1 - 3]. These devices operate essentially as two-terminal, non-volatile variable resistors. As such, they promise to revolutionize CMOS logic with respect to size, weight, and power by reducing the number of transistors required for memory and reconfigurable logic [4]. Unlike the many processing steps required to fabricate a transistor, memristive devices are often composed of as few as three material layers [5 - 7].

A typical memristive device has two critical resistance states, a high resistance state (HRS) and a low resistance state (LRS). To change a memristive device from the HRS to LRS (termed a SET operation), a voltage bias of the appropriate polarity and magnitude, V_{SET}, must be applied to the device. In practice, a current limit is usually imposed upon the device during a SET; otherwise, the unchecked high current through the device will permanently establish an LRS. Once the device is in the LRS, it may be returned to the HRS via a RESET operation, typically by applying a lower voltage, V_{RESET}, sans the current limit.

As may be expected from this description, several switching styles are observed in practice. When V_{SET} and V_{RESET} are of opposite polarity, the device is said to be bipolar. Furthermore, if V_{SET} = +V, then the device is said to be bipolar(+); else if V_{SET} = -V, the device is bipolar(-). When V_{SET} and V_{RESET} are of like polarity, the device is said to be unipolar. After the same fashion, if V_{SET} = +V, then the device is said to be unipolar(+); else if V_{SET} = -V, the device is unipolar(-). Should a device exhibit both

bipolar and unipolar switching, the device is said to be nonpolar. If all four bipolar and unipolar switching configurations are exhibited, the device may be said to be completely nonpolar.

Copper oxide is not a new material in the study of memristive devices [8-10]; however, a reliable copper-based memristive device remains of interest because of the already pervasive use of copper in CMOS circuitry. Several studies have used different means to create the Cu_xO layer including thermal oxidation [11], ion implantation [12], physical vapor deposition [13], and plasma oxidation [14]. Despite the various means to grow Cu_xO, it still remains a challenging material to work with because of interfacial voiding and poor thickness uniformity [13].

This paper examines the affects of varying POX reactive ion etch (RIE) power upon the properties of Cu_xO films. From the variations in the film properties, the affect certain physical parameters have upon subsequently fabricated Al/Cu_xO/Cu memristive devices can be isolated. Lastly, switching mechanism hypotheses will be compared to the experimental measurements.

2. Experimental

For this study, 1 μm of ECD Cu was grown atop a PVD Cu seed layer on a Ta/TaN/SiO_2/SiN/Si wafer. Cu_xO was prepared via a POX process at 0° C using a Trion Phantom III RIE system. This system allowed for two power settings, RIE and inductively coupled plasma (ICP) power. The ICP power generated high density plasma. The RIE power created a bias on the substrate to draw the free ions. Three samples were prepared for 10 min under 10 sccm O_2 at 45mT [14] where RIE varied from 100-300 W, while the ICP was fixed at 300 W. The final copper oxide thicknesses of each sample were determined by secondary ion mass spectrometry (SIMS); X-ray photoelectron spectroscopy (XPS) was used to determine the oxygen concentration in the aforesaid oxides. Finally, 400 nm thick Al top electrodes (TE), 195um diameter were patterned with a shadow mask, resulting in Al/Cu_xO/Cu memristive devices.

Characterization of the memristive devices was performed using sweep-mode voltage measurements using an Agilent B1500A Semiconductor Device Analyzer equipped with a probe station and thermal stage. Voltage sweeps progressed from 0V in ±10 mV steps. For all reported measurements, the Al TE was biased and an exposed Cu bottom electrode (BE) was grounded.

3. Results

3.1 Switching Devices

The copper oxide film thicknesses and copper/oxygen concentrations as determined by SIMS and XPS, respectively, are listed in Table 1. Cupric oxide, CuO, formed on the RIE 100 W sample; and on the RIE 300 W sample, the films were closer in stoichiometry to cuprous oxide, Cu_2O. While the oxide thickness did not monotonically increase with the RIE power, the oxygen concentration generally decreased with RIE power. Due to the nature of the oxide growth method and the non-stoichiometric nature of the RIE 200 and 300 samples, a non-negligible number of positively charged oxygen vacancies are expected [15]. As a result of these point defects , it follows that Cu_xO is a *p*-type semiconductor. The influence of these defects on the switching properties will be discussed in Section 5.1.

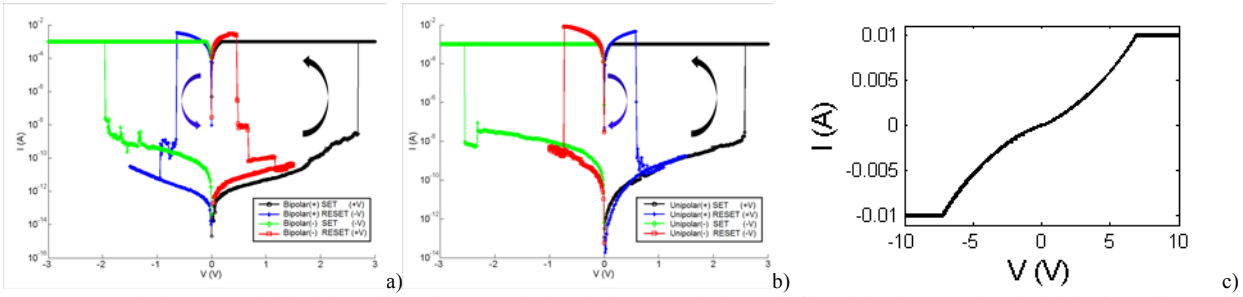
Table 1 Copper oxide thicknesses and copper/oxygen concentrations

RIE power (W)	Oxide thickness (nm)	Cu:O (atm.%)
100	42	50:50
200	618	55:45
300	488	60:40

Memristive devices from all three samples exhibited stable, complete nonpolar switching behaviors over repeated SET/RESET measurements. See Figure 1a) and 1b) for typical characteristic IV plots. A current compliance between 1-5 mA was required to limit the current during the SET process and ultimately prevent the devices from undergoing breakdown. Devices were cycled manually up to 40

cycles. In general, an initial forming step outside of normal operating parameters was not required unless a non-linear IV curve was observed in the HRS. This will be discussed in Section 5.1.

The operating parameters of these nonpolar devices are listed in Table 2. It is evident that neither the V_{SET} nor V_{RESET} values trended with the oxide thickness or oxygen concentration. Independent of the switching style and polarity, the switching voltages, V_{SET} and V_{RESET}, were consistent. In general, the LRS resistance was around 10 Ω; and the HRS resistances ranged from 2-40 k Ω.



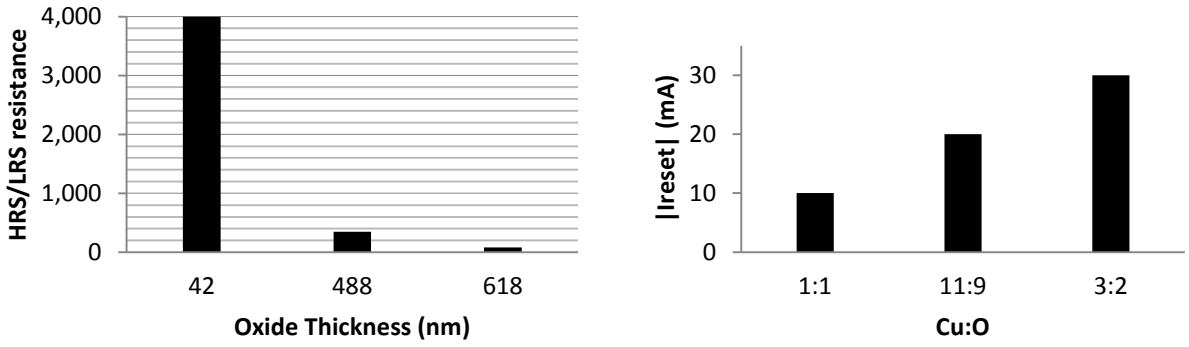
a) b) c)

Figure 1 Typical curves exhibited by Al/Cu_xO/Cu memristive devices. a) Bipolar switching behavior associated with both positive and negative device bias from RIE 300 W sample. b) Unipolar switching behavior associated with both positive and negative device bias for the same device tested in (a). c) Non-linear, non-switching memristive device from RIE 100 W sample

Table 2 Typical operative parameters for nonpolar memristive devices

RIE Power (W)	Oxide (nm)	$\|V_{SET}\|$ (V)	$\|V_{RESET}\|$ (V)
100	42	2.5-3	0.5
200	618	2-5	0.5
300	488	1.5-2.5	0.5

However, as is shown in Figure 2, the I_{RESET} and the HRS/LRS resistance ratio values did change depending upon the oxide composition and thickness, respectively. The ratio of the HRS/LRS resistances decreased with increasing oxide thickness, Figure 2 a). Since the LRS resistance was consistent among samples, this indicates that the HRS resistance was inversely proportional to the oxide thickness. Additionally, the required RESET current increased as the oxygen concentration decreased.



a) b)

Figure 2 a) relates the oxide thickness with the HRS/LRS resistance ratios, indicating a decrease in HRS resistance with oxide thickness. b) relates the Cu:O ratio with the required reset current, $|I_{RESET}|$, clearly indicating a inverse relation.

3.2 Non-switching Devices

For devices that did not switch, a non-linear IV curve generally symmetric about the origin was routinely observed, Figure 1c). This non-linear behavior is significant. 1) These devices could occasionally be switched at high negative voltages (-5 to -10 V) and using high current compliance values

(> |10 mA|). However, the subsequent switching voltages of these devices were less consistent; and the devices frequently stopped switching again. 2) When a typical nonpolar device failed (stopped switching), it always exhibited this non-linear behavior rather than the LRS or HRS.

3.3 Photolithography Challenges

An effort to measure the effect of contact size upon device behavior using a standard lift-off process to create variable TE sizes was undertaken; however, no viable devices were produced using this method. Any devices that did SET, spontaneously RESET within seconds, indicating limited memory functions. To help identify the source of this device failure, three samples from the same RIE 300 W wafer were each subjected to one of the three lift-off processing steps. Specifically, in the resist step, Shipley 1813 resist was applied to the first sample. During the baking step, the second sample was subjected to 110° C for 5 min and 90° C for 1 min. The final sample was exposed to 365 nm UV light for 12 sec. Al TE were deposited through a shadow mask via e-beam deposition.

The samples exposed to the heating step and the UV step exhibited resistive switching properties similar to the viable devices described above. The sample subjected to the resist did not demonstrate any switching. This indicates that application of photoresist negatively affected device switching behavior. This detrimental effect resulted from either poor electrical contact between the Al and Cu_xO layer due to inadequate cleaning or a chemical reaction between the resist and one of the materials in the film stack.

4. Theory

Several methods for conduction have been proposed for Cu_xO memristive devices. Electrode material dependant conduction variability in the HRS suggests an interfacial mechanism [16]. For conduction in the HRS, space-charge-limited-current (SCLC) [8] has been reported as well as Schottky emission [17] and the Poole-Frenkel effect (PF) [14].

There are several methods for identifying the dominant conduction mechanism in a memristive device based on IV measurements. For Ohmic conduction, which follows $V = IR$, the slope, m, of the curve on a double logarithmic IV plot would be $m = 1$. Should the slope change to $m = 2$ (Child's Law, $I \alpha V^2$) and even higher values as V increases, this generally indicates SCLC. SCLC describes the situation where unfilled traps inhibit electron conduction. Once all the trap sites are filled, electron flow is no longer trap-mediated, corresponding to a large increase in current [18].

Other non-linear conduction mechanisms are Schottky emission and the Poole-Frenkel (PF) effect. Schottky emission describes electrical conduction resulting from electric field-induced lowering of the energy barrier at the interface of a metal and an insulator (or semiconductor) as a result of differing work functions. This effect may be described as [19]

$$\ln(J_S) = \frac{1}{2kT}\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}}\sqrt{E} + \left[\ln(A^*T^2) - \frac{q\phi_s}{kT}\right], \tag{1}$$

where Js is the current density, q is the electron charge, ε_0 is the permittivity of free space, ε_r is the dielectric constant of the material, k is Boltzmann's constant, T is the Kelvin temperature, E is the electric field, A^* the Richardson constant, and ϕ_s is the barrier height. Based on (1), Schottky emission is the dominant conduction mechanism when a plot of $\ln(I)$ vs. $V^{1/2}$ results in straight line.

The PF effect describes the emission of electrons from trap states in a material as a result of the reduced thermal energy requirements in the presence of a high electric field [19],

$$\ln\left(\frac{J_{PF}}{E}\right) = \frac{1}{\xi kT}\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}}\sqrt{E} + \left[\ln(C) - \frac{q\phi_s}{\xi kT}\right], \tag{2}$$

where C is a proportionality constant and ξ is a constant between 1 & 2. For $\xi = 1$, the equation is the standard PF equation. However, $\xi = 2$ if the dielectric contains a significant number of trap sites; and thus, (2) becomes the modified PF equation, which is more Schottky like than the standard PF equation. Similar to above, plotting $\ln(I/V)$ vs. $V^{1/2}$ will result in a linear relationship if the device conduction is principally from the PF effect.

5. Discussion

5.1 Conduction Method Analysis

Fitting these equations to both switching and non-switching devices is useful for determining the switching mechanism. As can be seen in the double logarithmic IV plots in Figure 3, Ohmic conduction is clearly indicated as the dominant conduction mechanism for both the LRS and HRS over both SET, Figure 3a), and RESET, Figure 3b), operations. Ohmic conduction during LRS is often attributed to filament formation of a conductive species [9, 14]. Ohmic conduction in the HRS is an unexpected result. Given the drastic resistance change during SET, a conductive channel is not expected in the HRS. However, for such devices, neither the Schottky emission nor the PF effect tests indicated an alternative HRS conduction method (not shown).

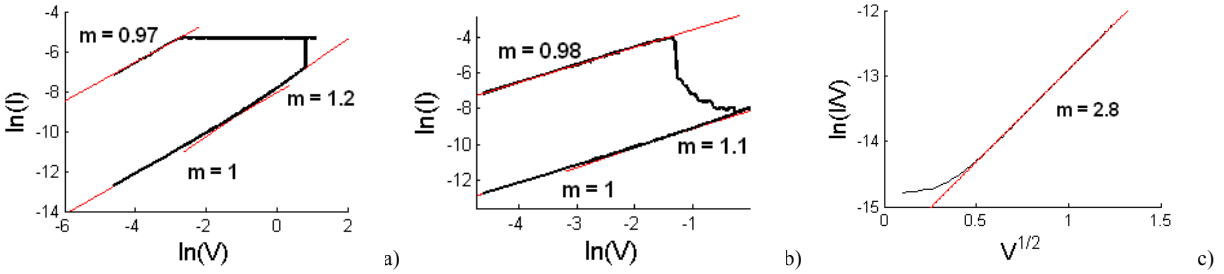


Figure 3 Double logarithmic IV plot of a RIE 300 W bipolar(+) device. Ohmic conduction is clearly indicated by the slopes of the curves as the dominant conduction method for both LRS and HRS. a) shows the IV for the SET operation. b) is for the RESET. c) indicates PF effect conduction at high voltages.

An Ohmic contact can form between a *p*-type semiconductor and a metal with a deep work function, else a Schottky contact will result [20]. Given the work function of Cu_2O (4.84 eV), both Cu (4.35 eV) and Al (4.25) should form Schottky contacts as fabricated. Since this is not observed, some phenomenon is likely modifying the interfacial regions. Oxidation of the Al TE has been reported before though the specific affects have not been established [21]. High dopant or defect state concentrations may also significantly alter contact properties [22].

However, in some switching devices the HRS conduction mechanism changed with the voltage. At first, again, at low voltages, Ohmic conduction is observed, but at high voltages (>1.5 V), Poole-Frenkel effect conduction is indicated, Figure 3c). This suggests a non-negligible number of trap states are inhibiting electron conduction, but switching is not the result of merely filling the trap states as described by SCLC.

For non-switching devices of IV behavior similar to Figure 1c), the conduction mechanism also changes with the voltage. Using the double logarithmic plot shown in Figure 4a), it is again clear from the slope that Ohmic conduction is the principle conduction method at low voltages. At higher voltages, however, the slope is decidedly non-linear. While the curve may be fit with multiple lines to suggest SCLC conduction, Figure 4a), the transition points are typically better defined, as shown in [23, 24]. There is a lack of strong linearity when the same points are graphed as $\ln(I)$ vs. $V^{1/2}$ (not shown), which is not a strong indication of Schottky conduction either. Finally, there is marked linearity in the PF test plot, $\ln(I/V)$ vs. $V^{1/2}$, Figure 3 b), indicating this as the primary conduction method at high voltages. Because both switching and non-switching devices may use the same conduction mechanism, there is likely an additional physical parameter not identified in this study that governs whether a device switches or not.

To further analyze LRS conduction mechanism, RIE 300 W devices that had been SET were measured at elevated temperatures. Decreasing LRS resistance during heating of a SET device generally indicates that the conduction path is predominantly a semiconductor; whereas, increasing LRS resistance indicates a metallic conduction path. For these devices, the LRS resistance decreased 17% on average from 20° C to 145° C (not shown). These data suggest that it is unlikely that a metallic filament is present in the LRS.

5.2 Switching Mechanism Analysis

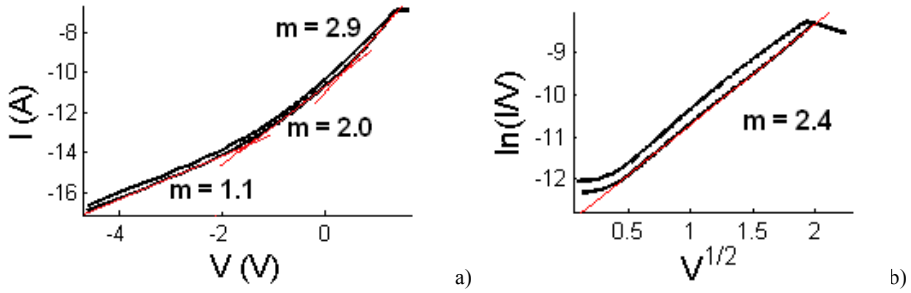


Figure 4 Conduction mechanism test of non-switching devices. a) clearly indicates Ohmic conduction at low voltages. SCLC type fits may be imposed on the curve, but the transition points are not well defined. b) clearly indicates Poole-Frenkel emission.

In similar works, the movement of oxygen atoms forming a conductive filament was suggested as the cause of the SET operation. Then upon a later sweep, the increased current would rupture the filament due to Joule heating [14]. It was later shown that the Al/Cu_xO interface, a CuAlO layer, formed and acted as the primary switching layer [21].

A unique property of the devices fabricate in this research is the complete nonpolar switching behavior. Complete nonpolar switching is not frequently reported in memristive devices, rather a device exhibits either bipolar or unipolar switching. While bipolar switching may be readily attributed to ion movement, the very similar $\pm V_{SET}$ values observed in this study suggest that (1) the SET mechanism is either polarity independent or (2) there are two separate polarity dependant mechanisms present that are activated by similar voltage magnitudes. The RESET mechanism could readily be attributed to Joule heating due to high current flow, which is inherently polarity independent. While filament creation/rupture is not incompatible with the observed data, the Ohmic contacts and semiconductor conduction path require further study. Understanding the physical differences between the switching and non-switching devices will likely be required to answer this conclusively.

6. Conclusion

The effects of RIE power upon CuxO film properties and their subsequent effect upon Al/Cu_xO/Cu memristive devices has been studied. Increasing RIE power was inversely proportional to the oxygen concentration of the resulting Cu_xO film. Oxide thickness also tended to increase with increasing RIE power. The resulting Al/Cu_xO/Cu memristive devices all demonstrated complete nonpolar switching. Device analysis showed an inverse relation between oxide thickness and HRS/LRS resistance ratios & an inverse relation between oxide oxygen concentrations and required RESET currents. The conduction mechanism of these devices was Ohmic over LRS for all devices via a semi-conducting conduction path. Over HRS for viable devices, either Ohmic or Poole-Frenkel effect conduction were observed. For devices that do not switch, HRS conduction appeared to fit the PF effect equation. The exact nature of the switching mechanism and the physical difference between switching and non-switching devices cannot be conclusively determined from the available data at this time.

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